

# Appendix A.

## Global Voltage Range Plots for Generic Feeder Voltage Regulation Analysis Cases

This appendix provides plots of the global maximum and minimum voltage results for each voltage regulation case performed using the generic radial feeder models, as a function of DG penetration. The global maximum and minimum voltages are the maximum and minimum primary voltages anywhere on the feeder, for either peak or minimum system loading. The global maximum and minimum for each case are usually not for the same location nor the same load level. These plots summarize the overall voltage regulation performance, and clearly indicate the DG penetration level where voltage regulation issues become significant.

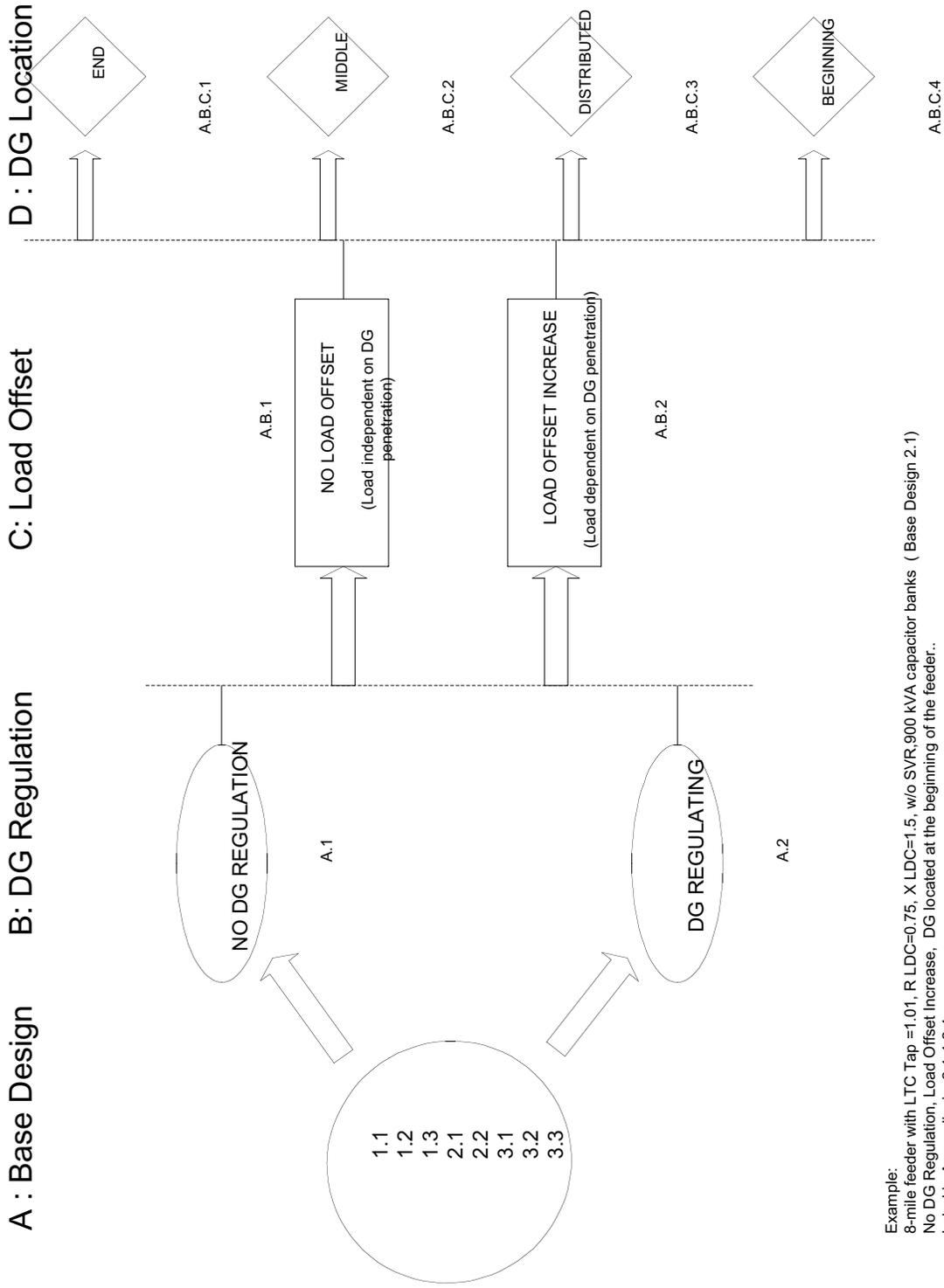
The solid lines in the global voltage range plots indicate the range for the DG operating at 100% of capacity. Because the DG might operate at any power level between 0% and 100%, the full voltage range must also include voltages where the DGs are not generating. This is equivalent to the voltage range at 0% DG penetration. Where the voltage range for 0% DG output is outside of the range for 100% output, then the extended range is shown by broken lines in the plots, labeled reference max and reference min .

### Case Key

A total of 128 sub-cases were performed, as indicated by the case tree structure illustrated on the following page. Within each sub-case, loadflow analyses were performed for two load levels and six DG penetration levels in order to generate the global voltage range plots shown in this appendix. Thus, a total of 1,536 individual loadflow cases were performed.

The case tree structure shown on the next page indicates the sub-case numbering scheme used to identify voltage range plots in this appendix. Also, each plot has a label which can be interpreted as follows:

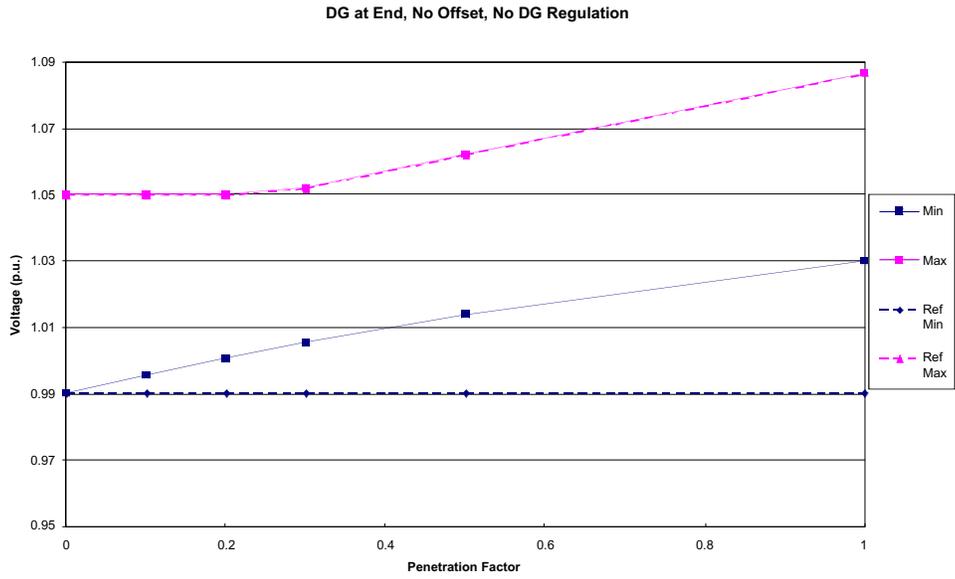
1. **DG Location** ( DG at End, DG at Middle, DG at Beginning, DG Distributed, self-explanatory)
2. **Load Change Scenario** ( No Offset feeder load independent of DG penetration, Offset Increase — feeder peak load increased an amount equivalent to DG capacity)
3. **DG Voltage Regulator Implementation** ( No DG Regulation, DG Regulating refer to whether the DG reactive power output is controlled to regulate the local bus voltage)



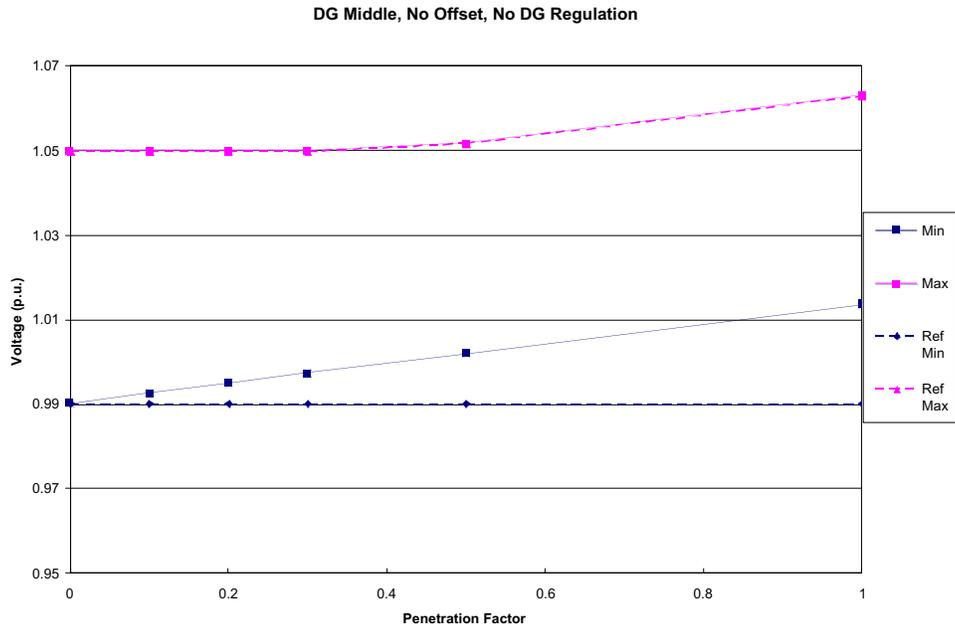
Example:  
 8-mile feeder with LTC Tap =1.01, R LDC=0.75, X LDC=1.5, w/o SVR,900 kVA capacitor banks ( Base Design 2.1)  
 No DG Regulation, Load Offset Increase, DG located at the beginning of the feeder.  
 Label in Appendix is 2.1.1.2.4

# BASE DESIGN 1.1

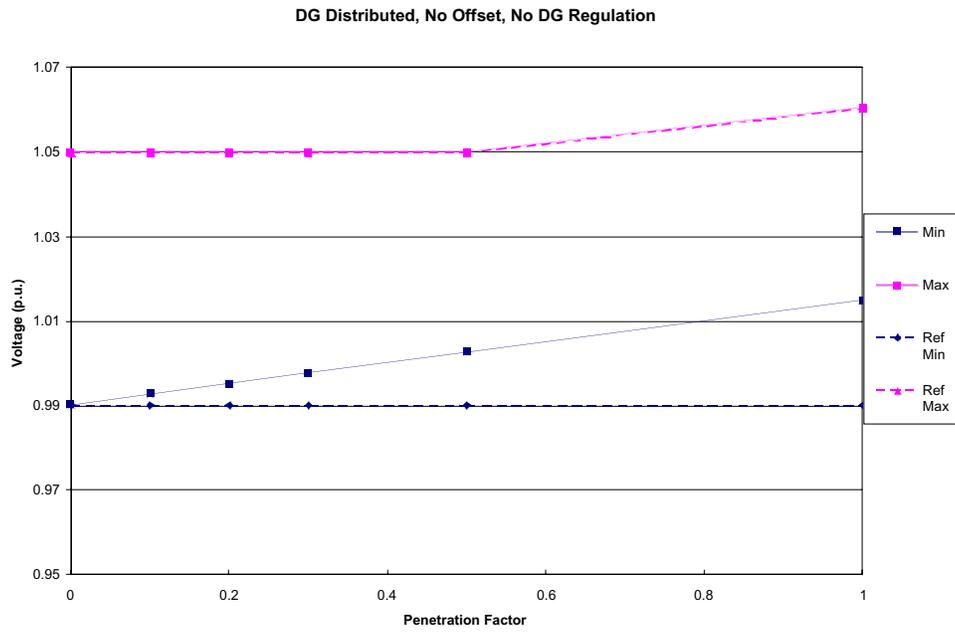
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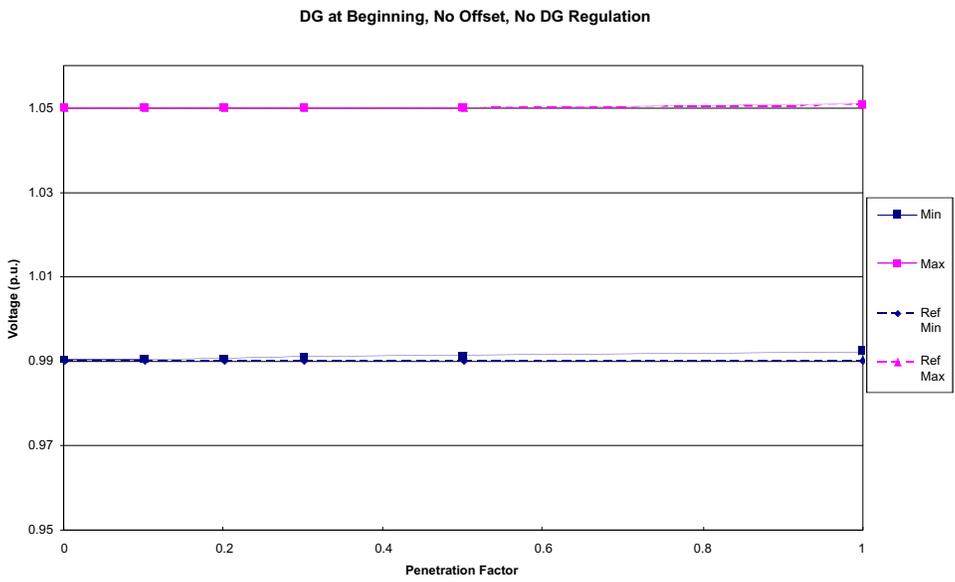
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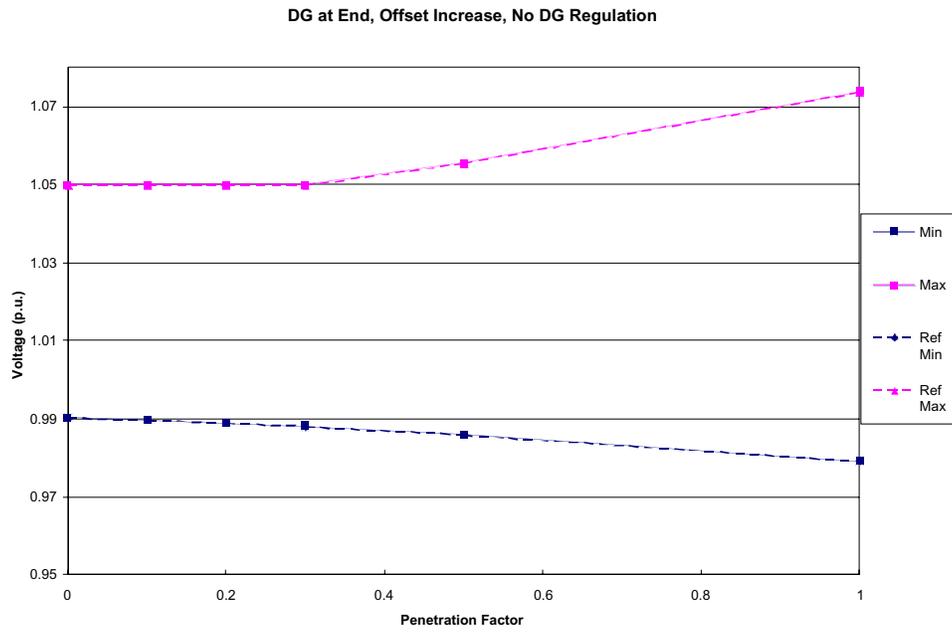
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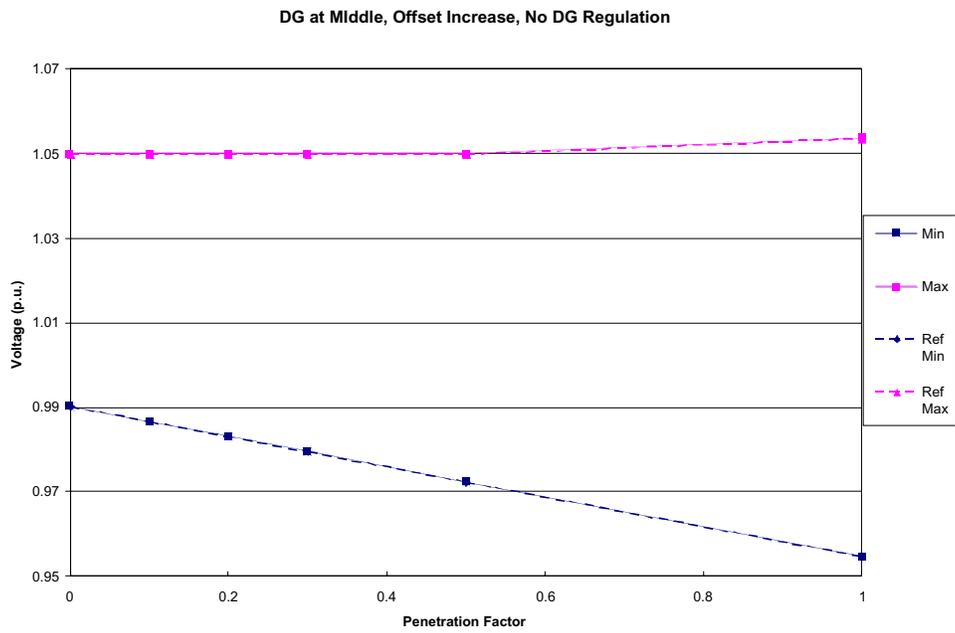
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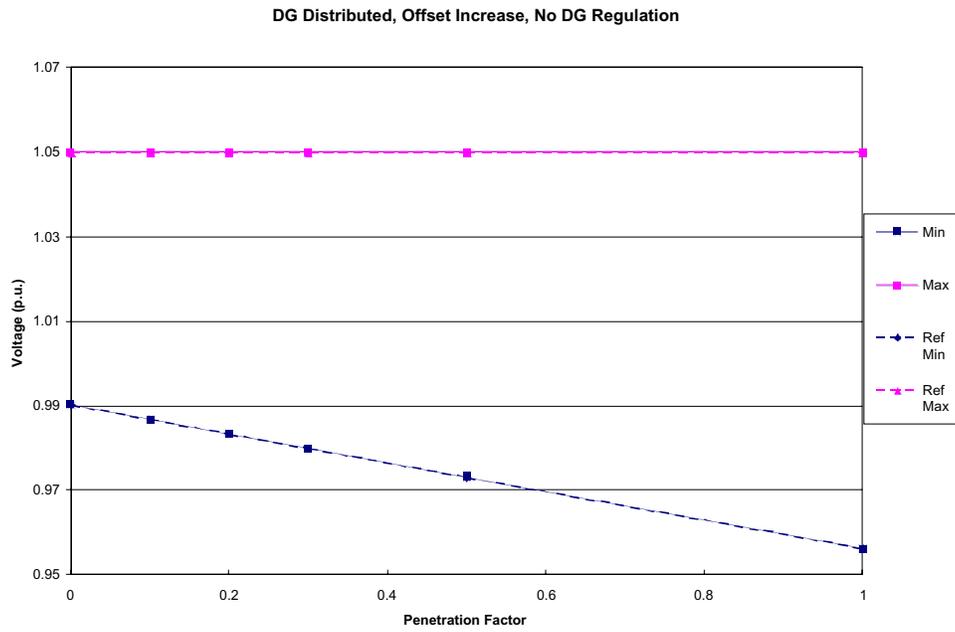
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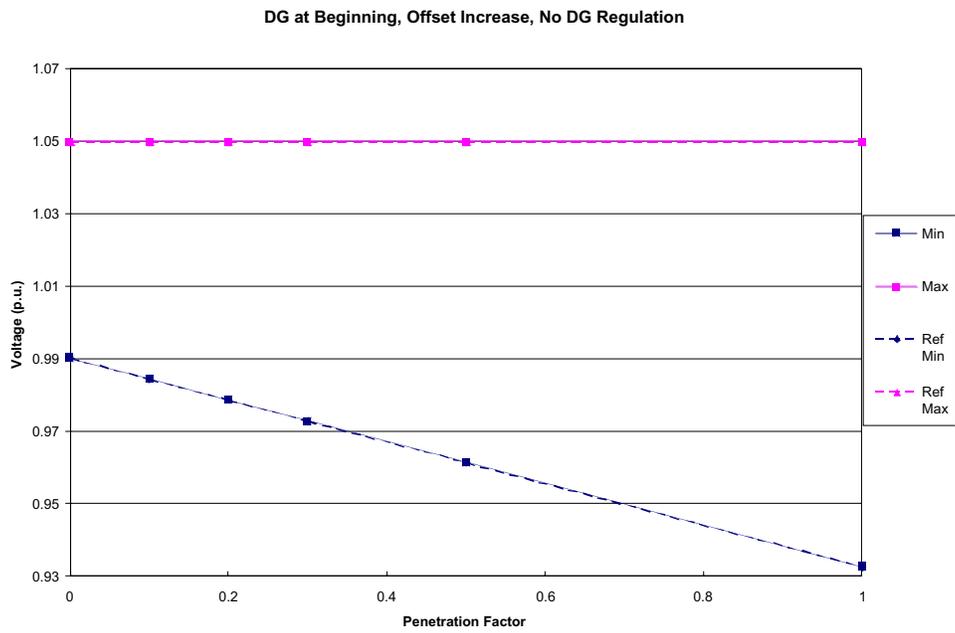
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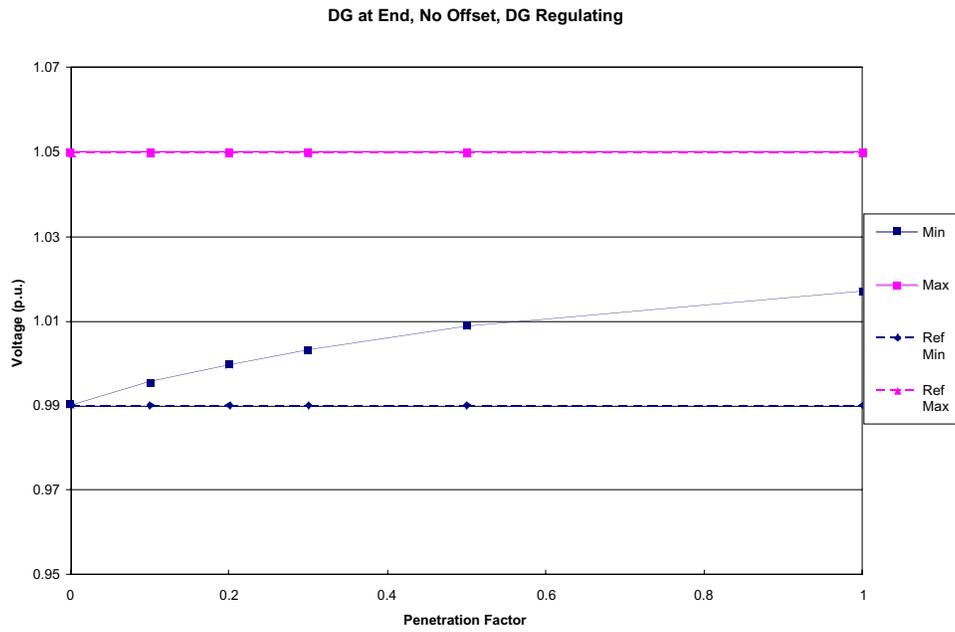
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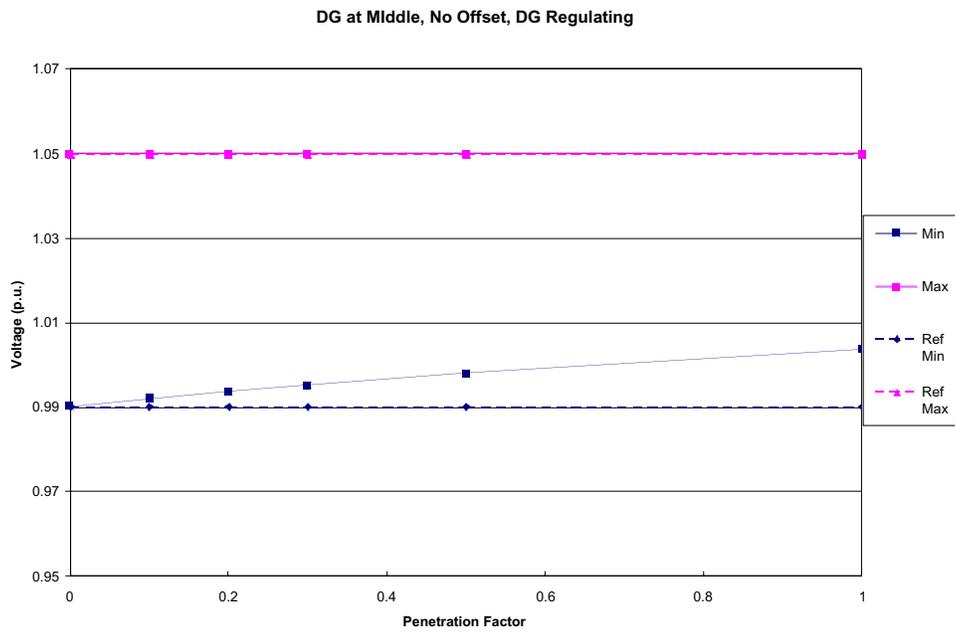
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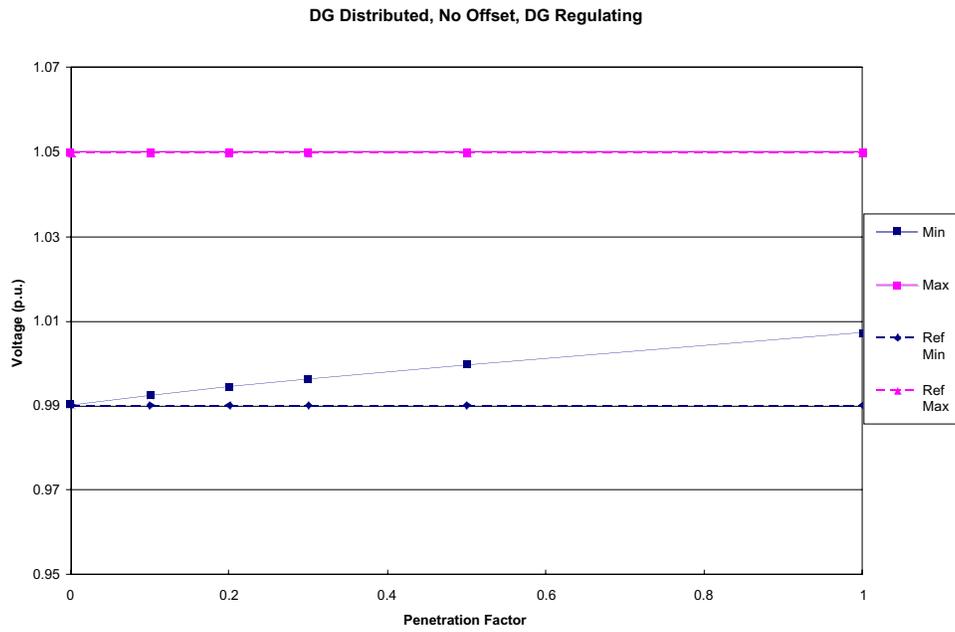
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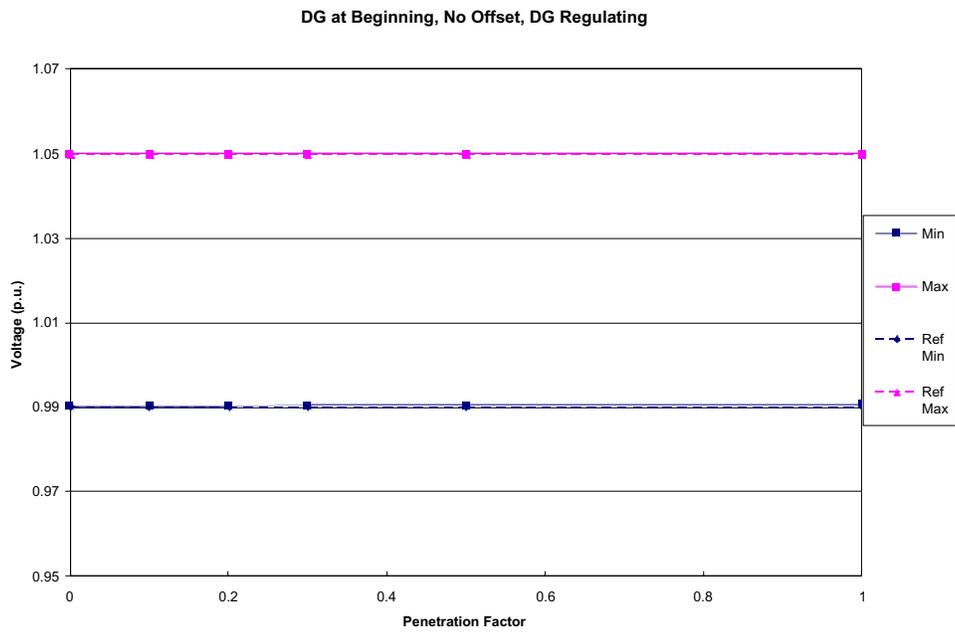
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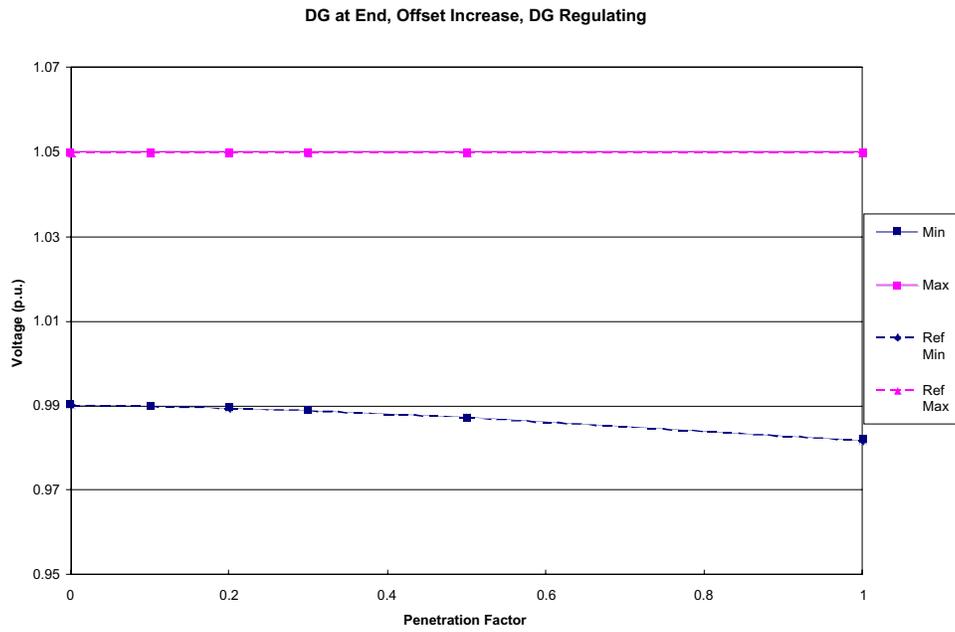
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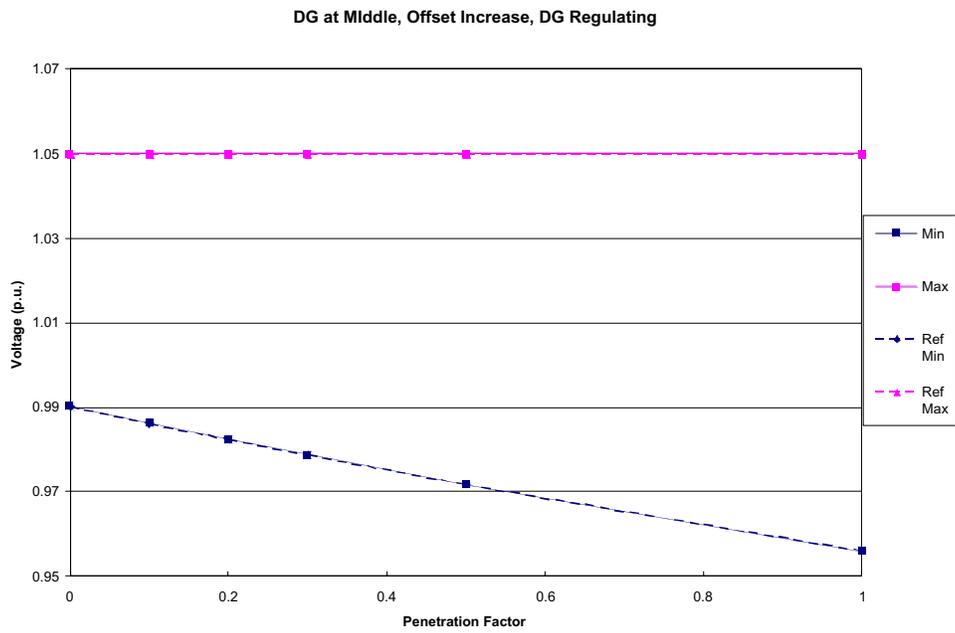
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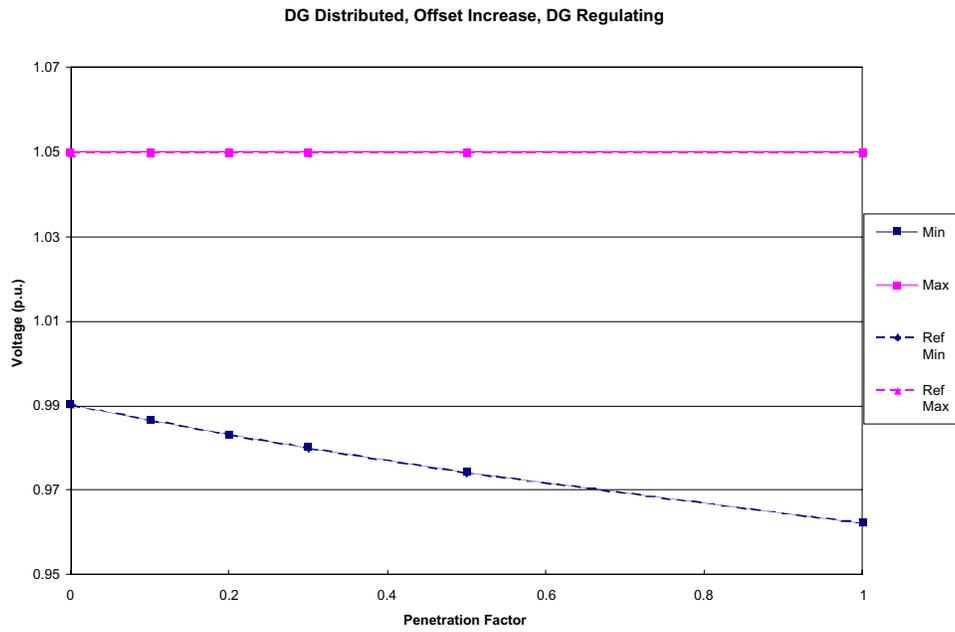
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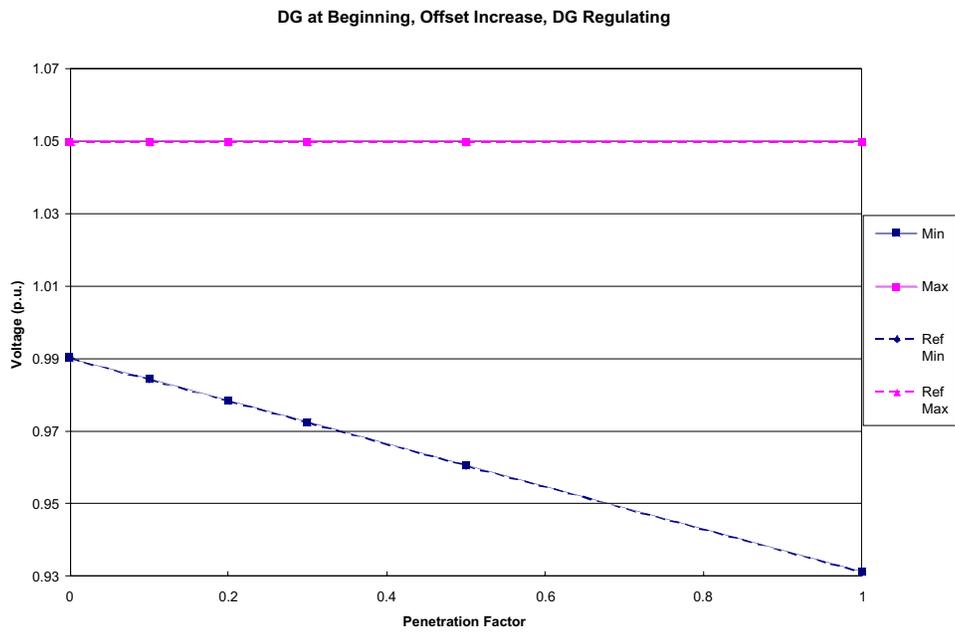
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### 1.1.2.2.3

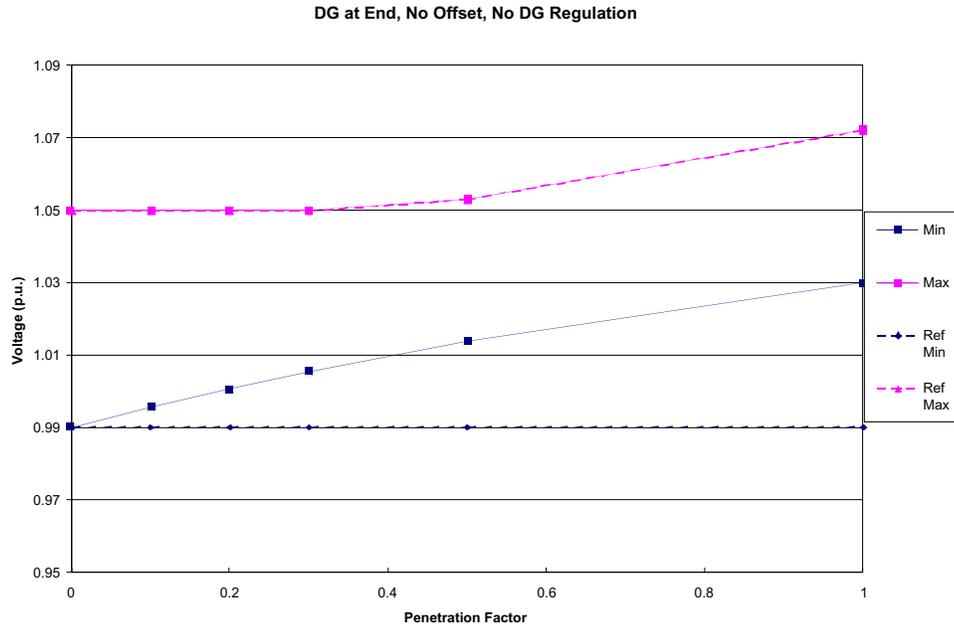


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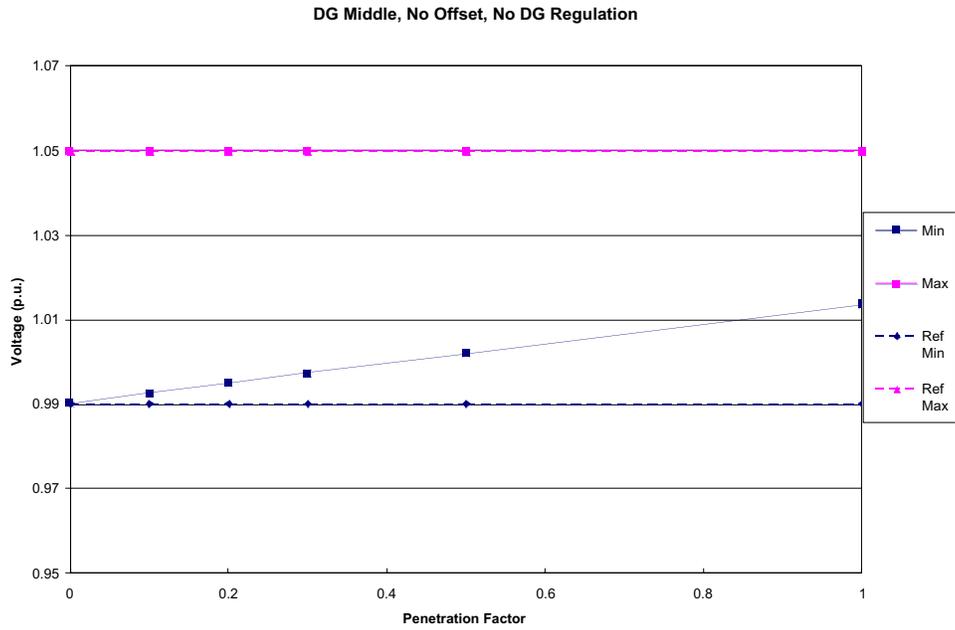


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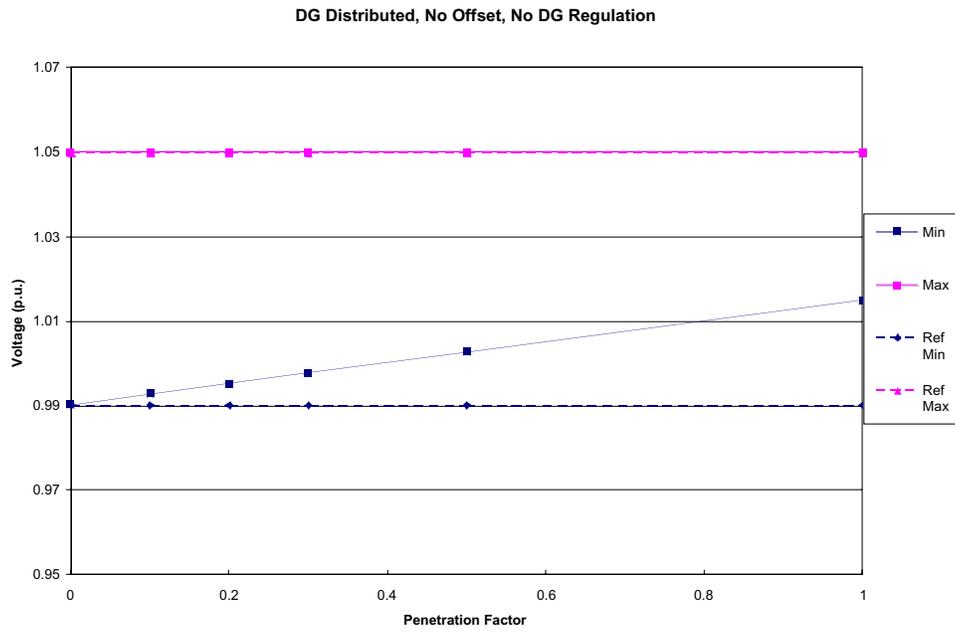
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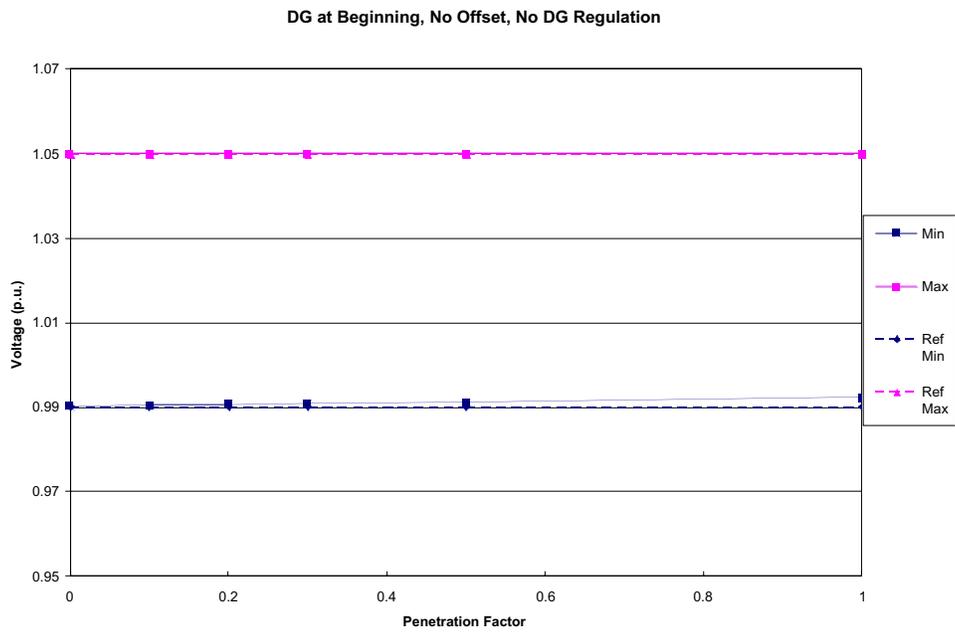
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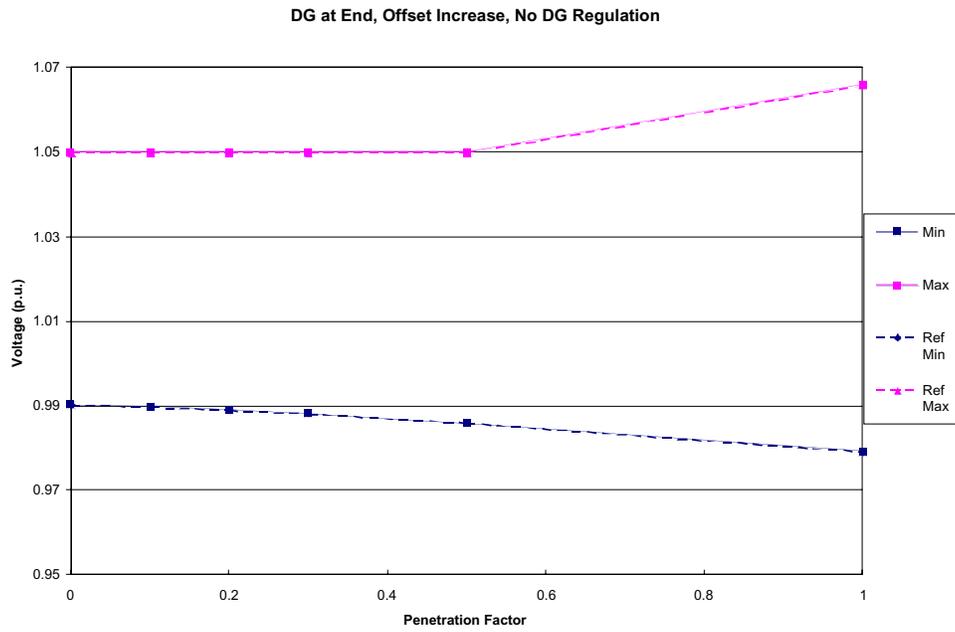
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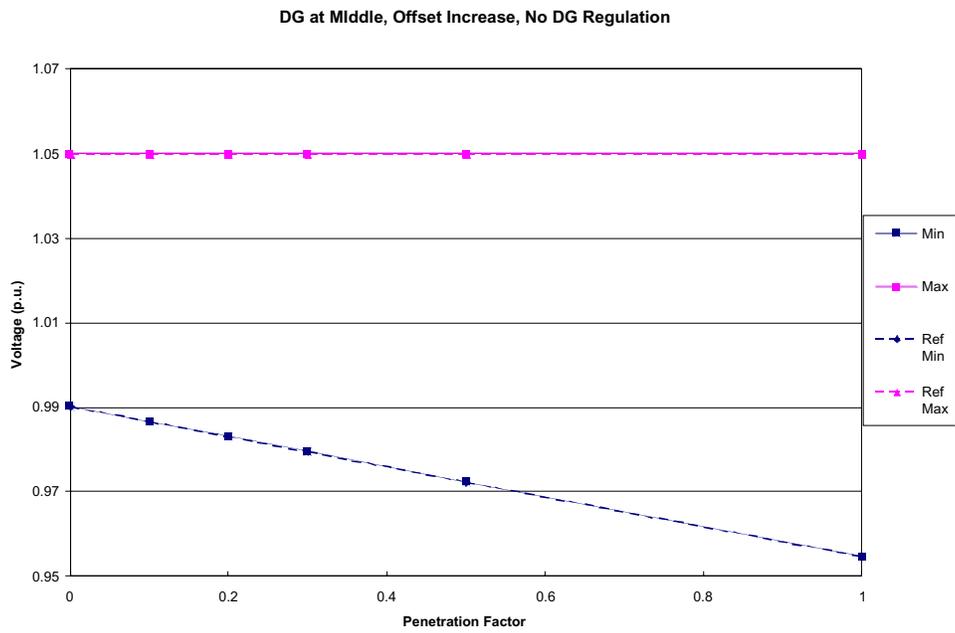
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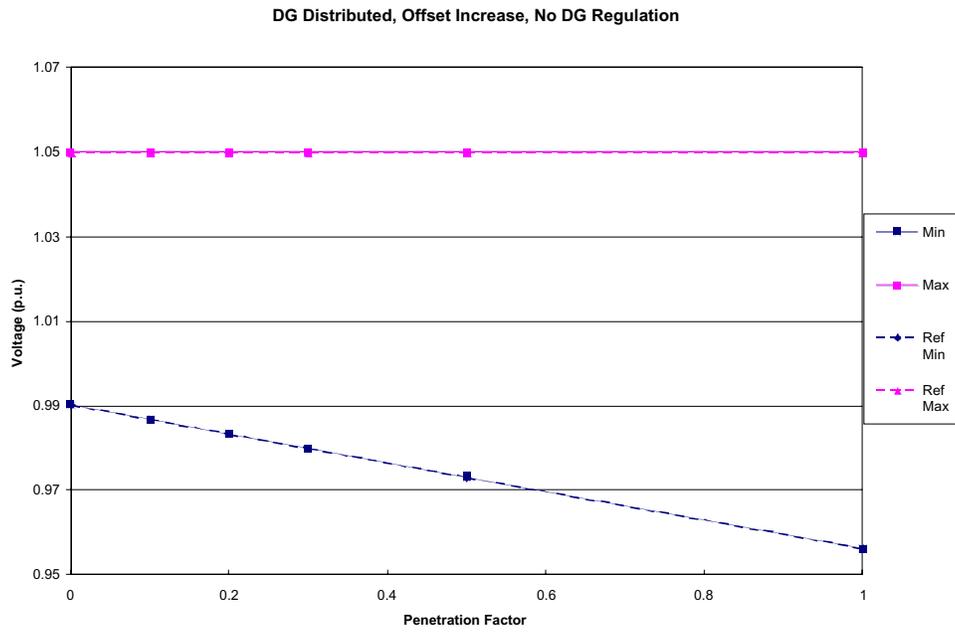
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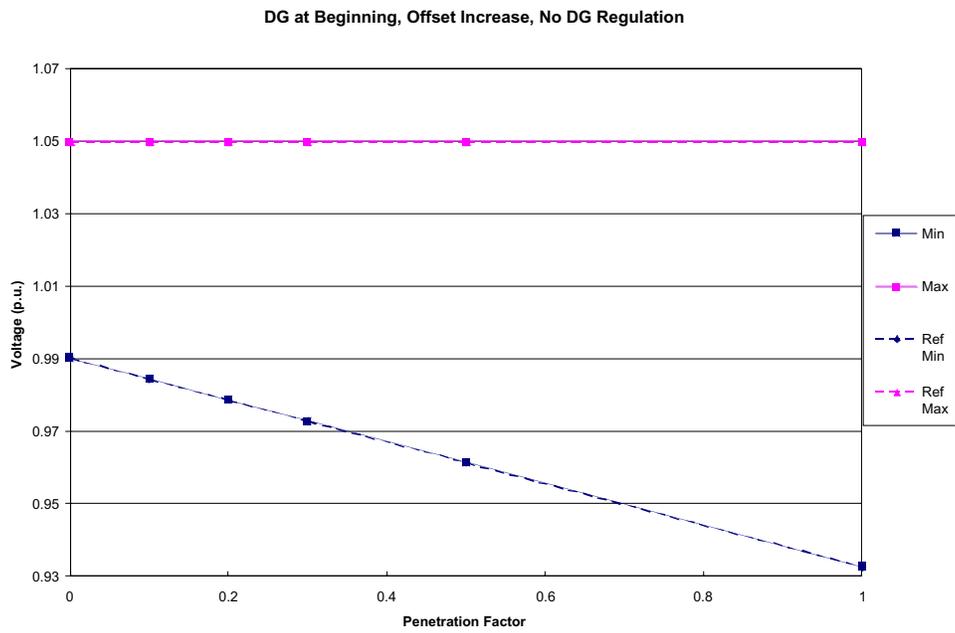
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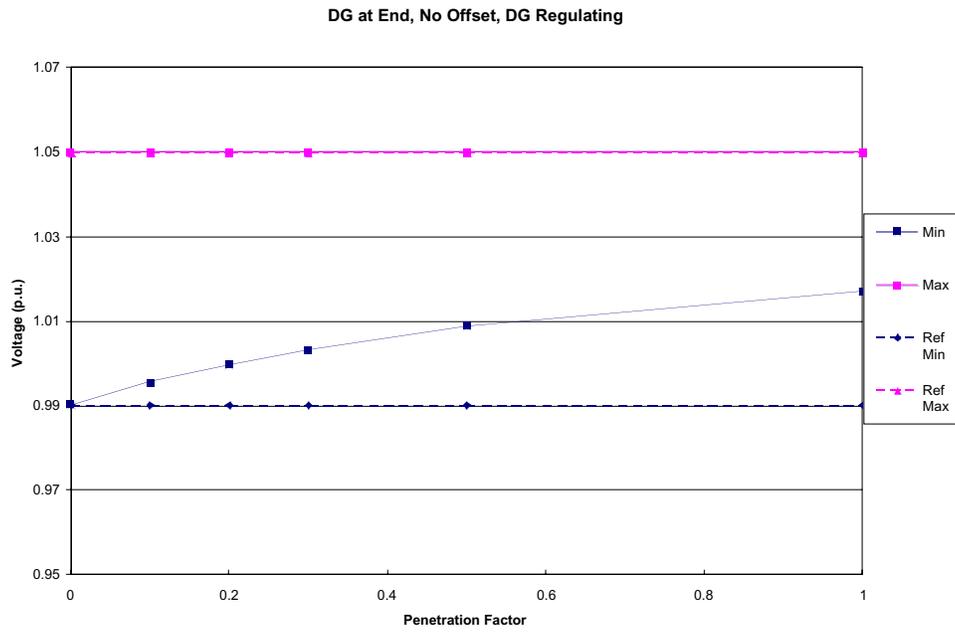
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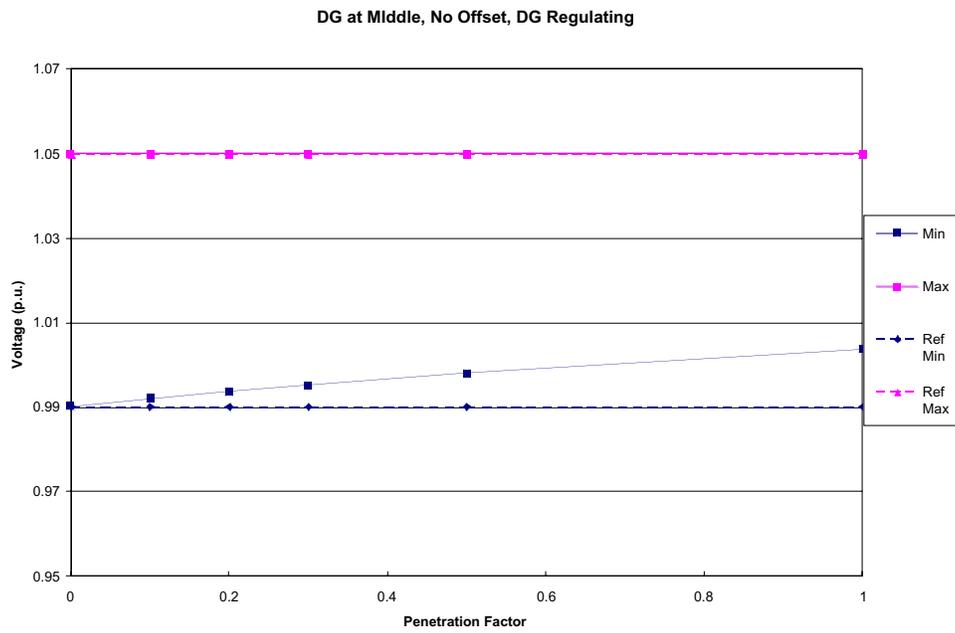
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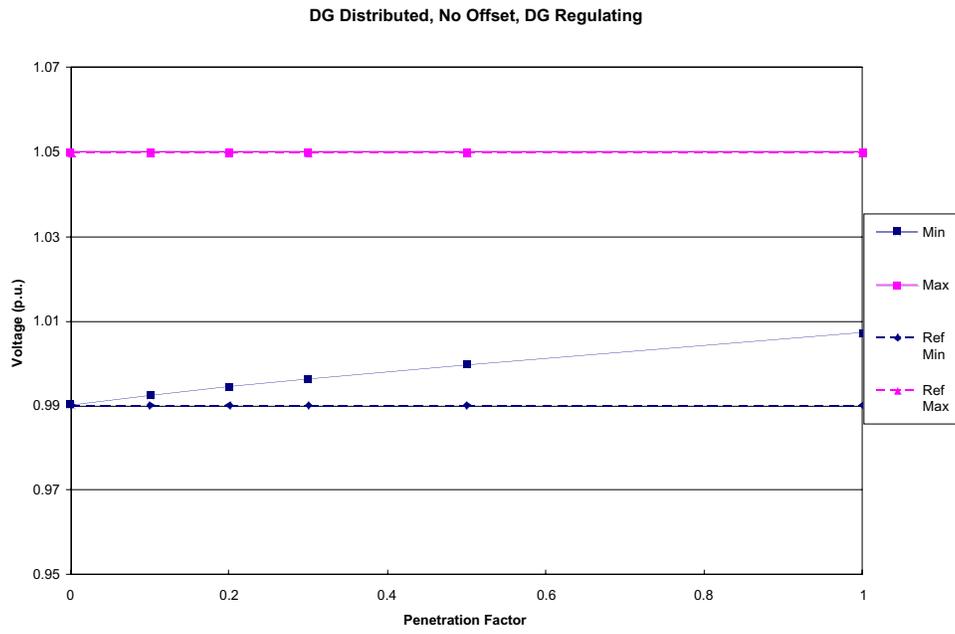
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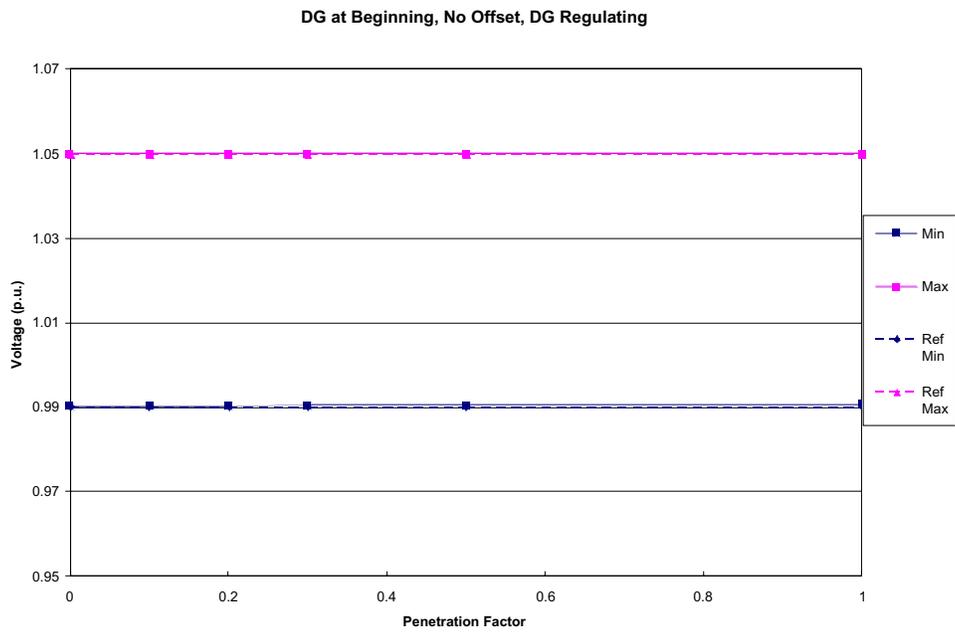
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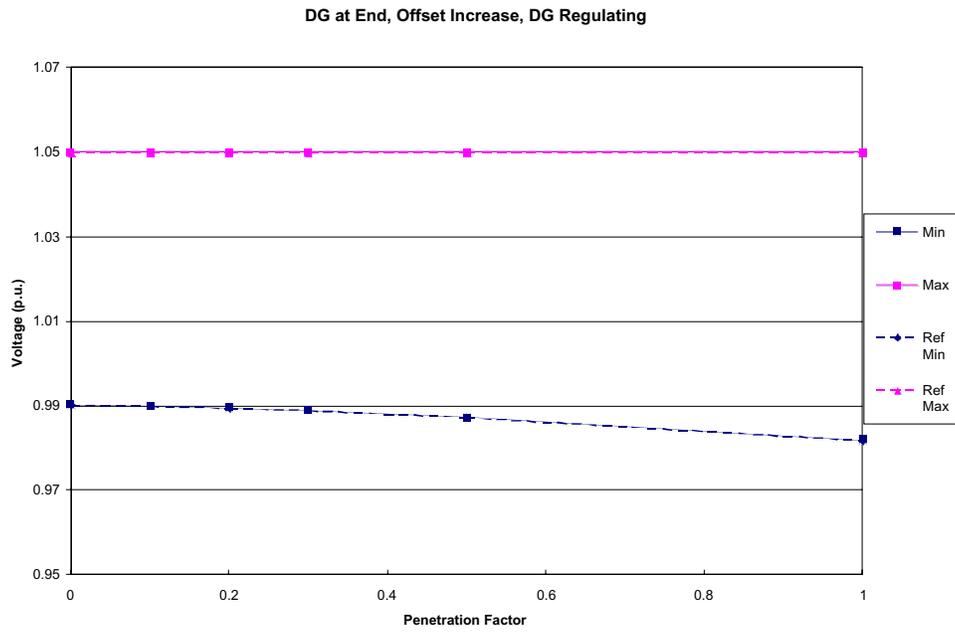
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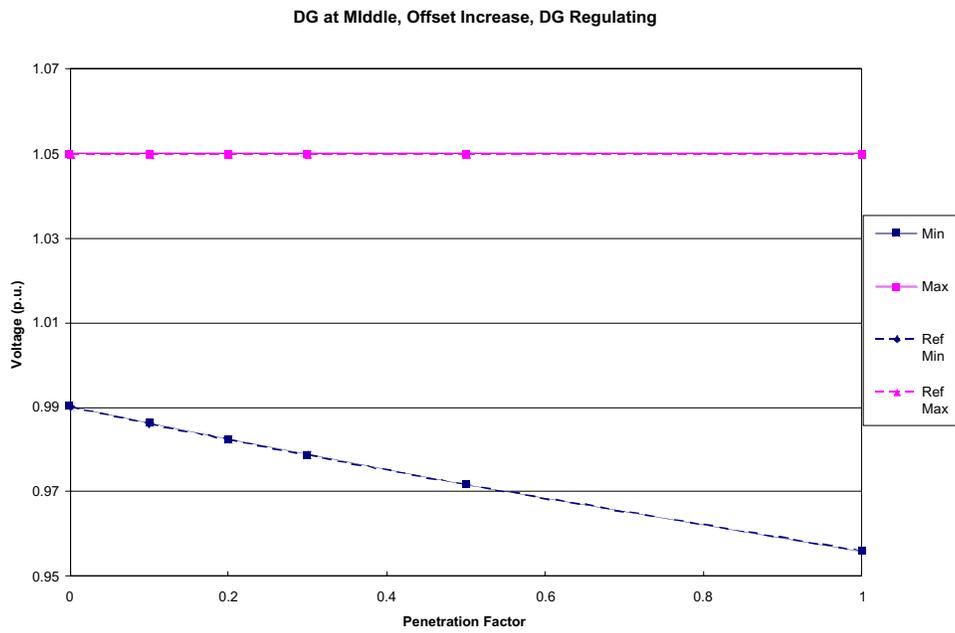
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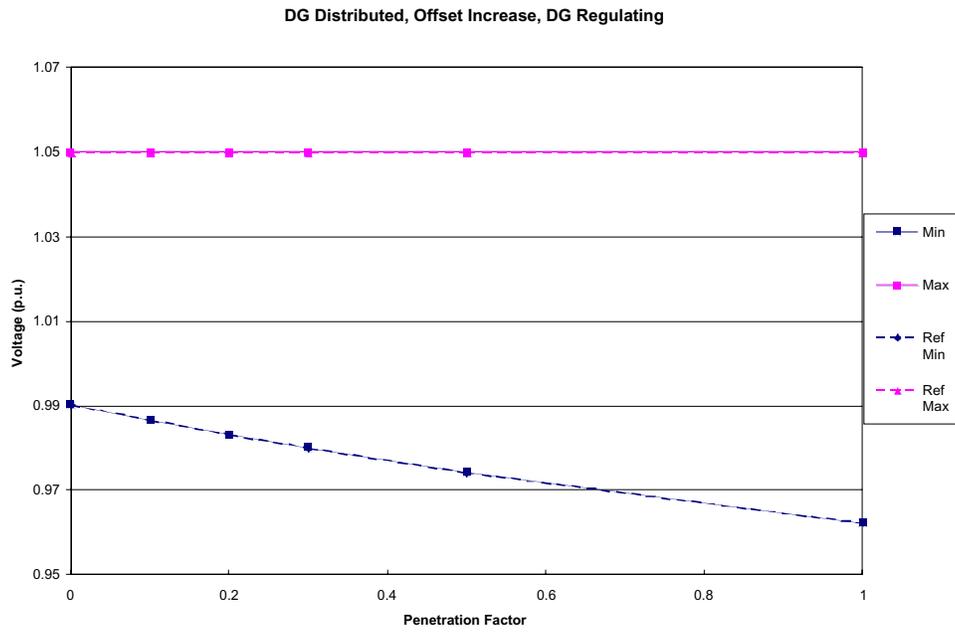
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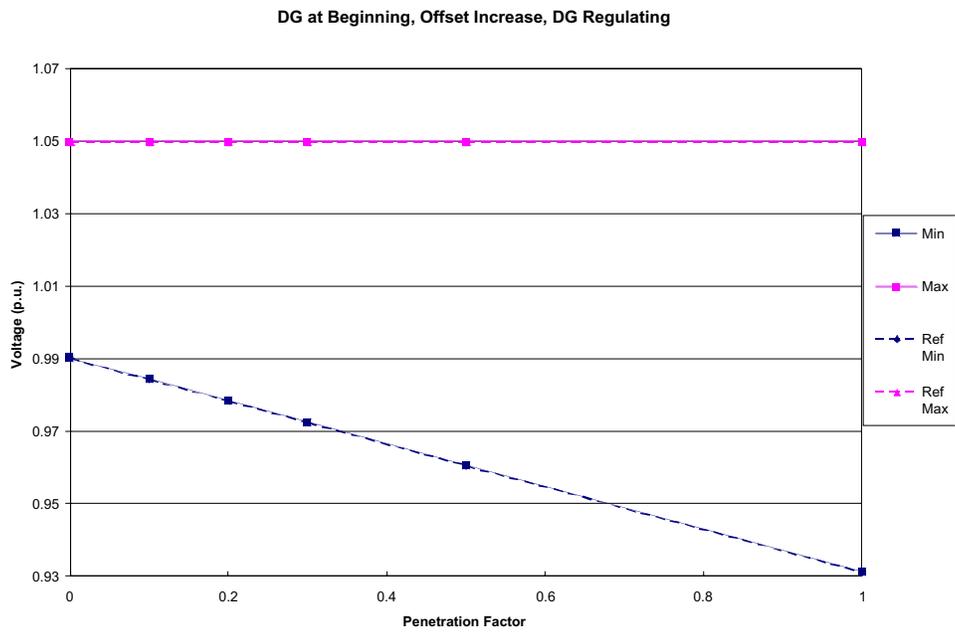
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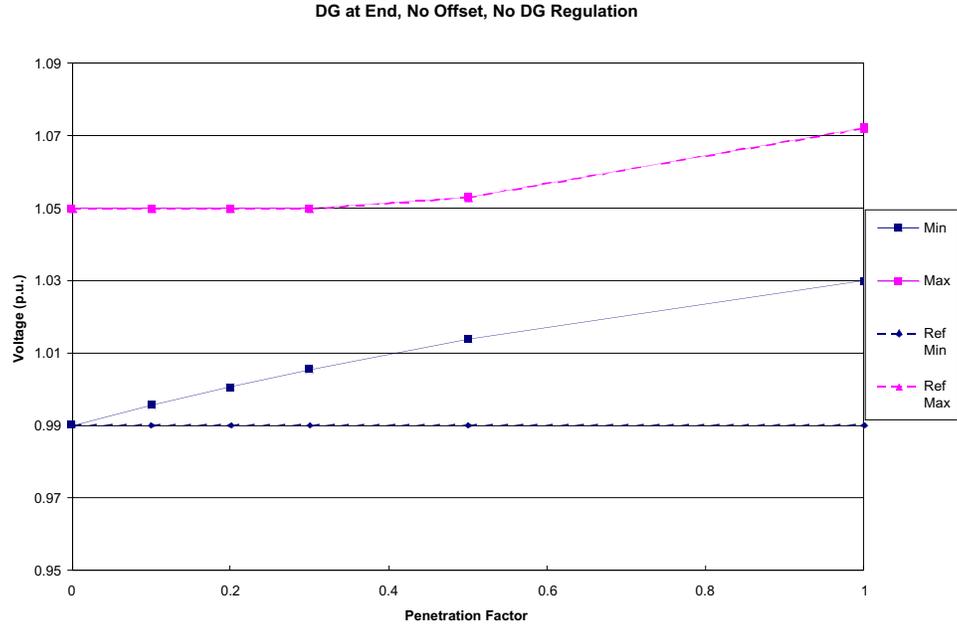


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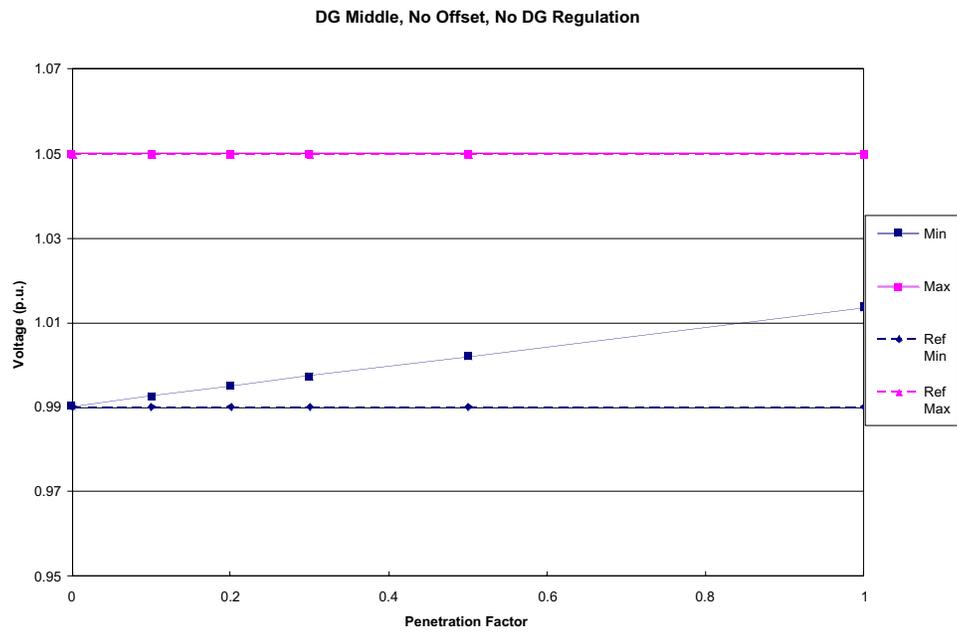


# BASE DESIGN 1.3

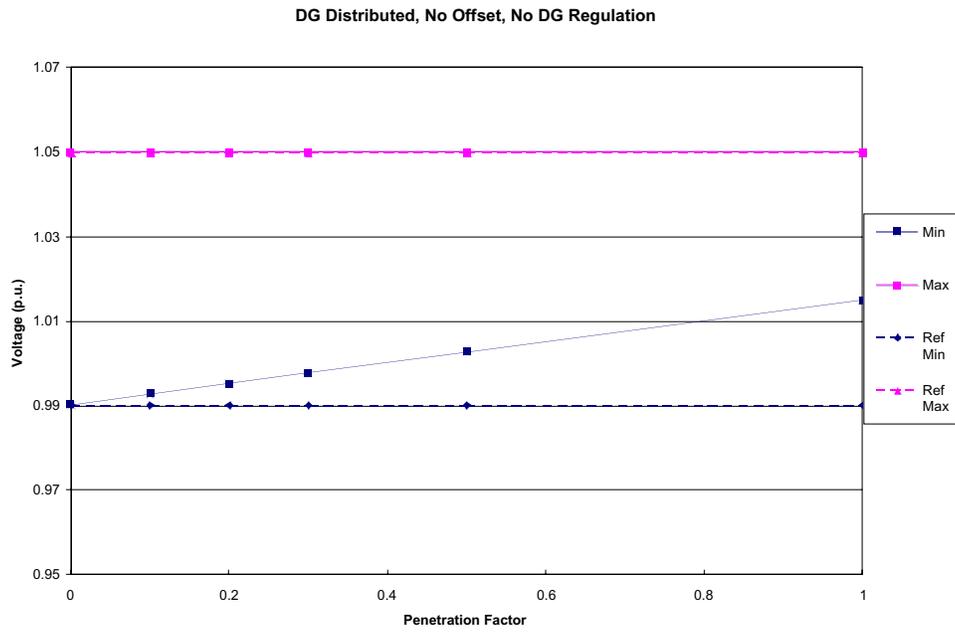
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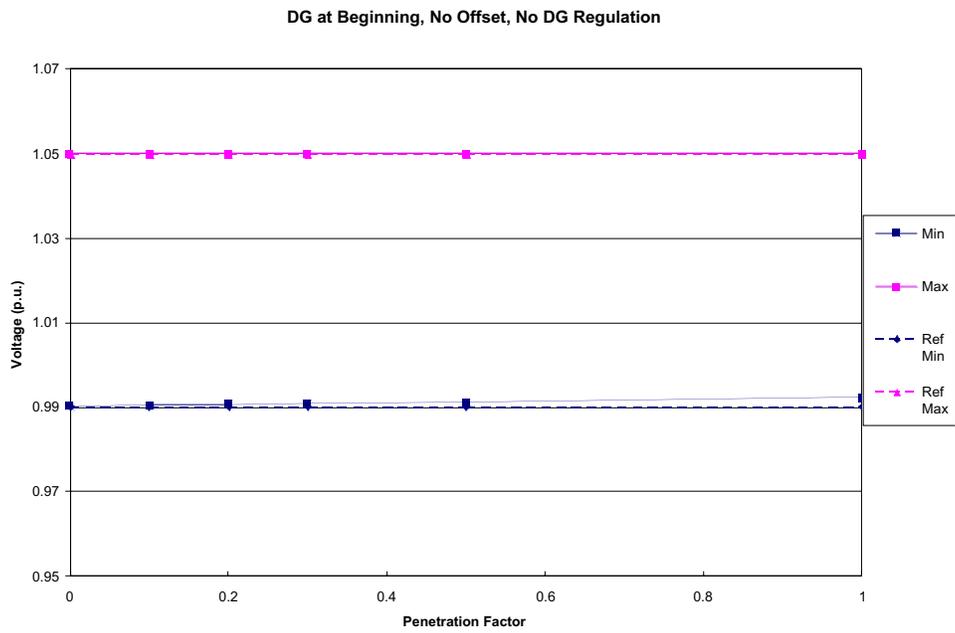
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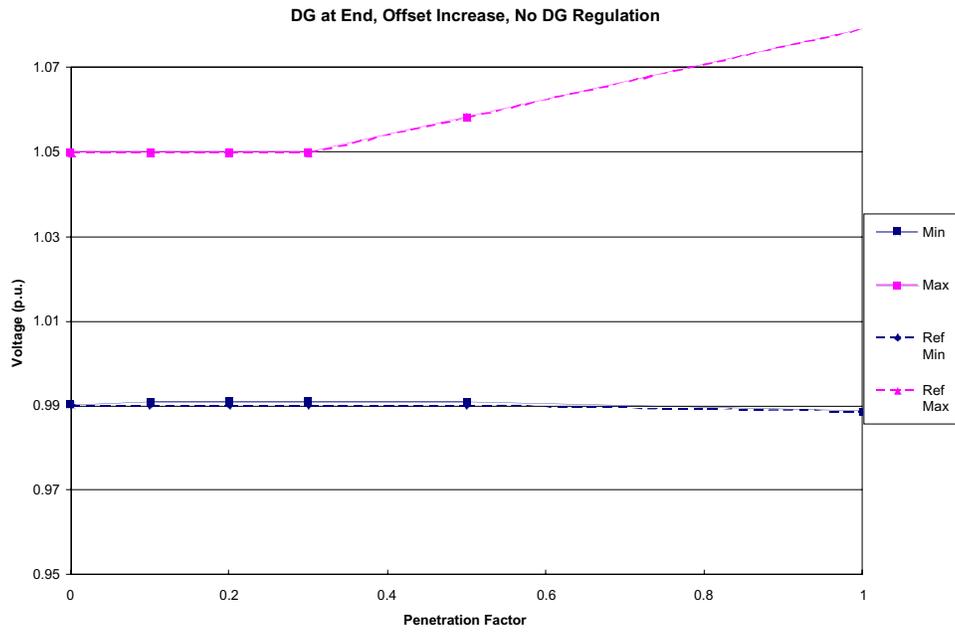
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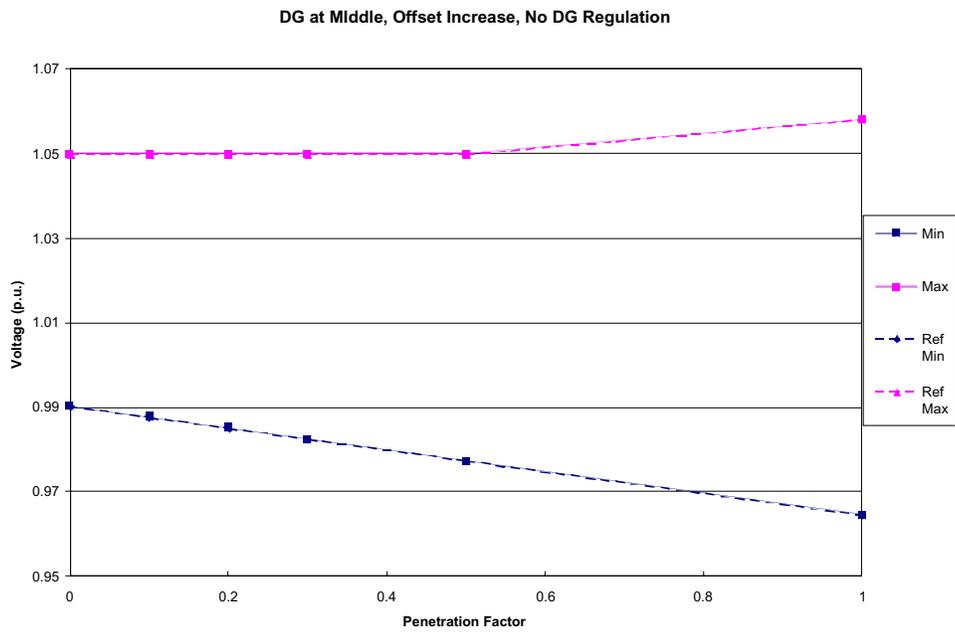
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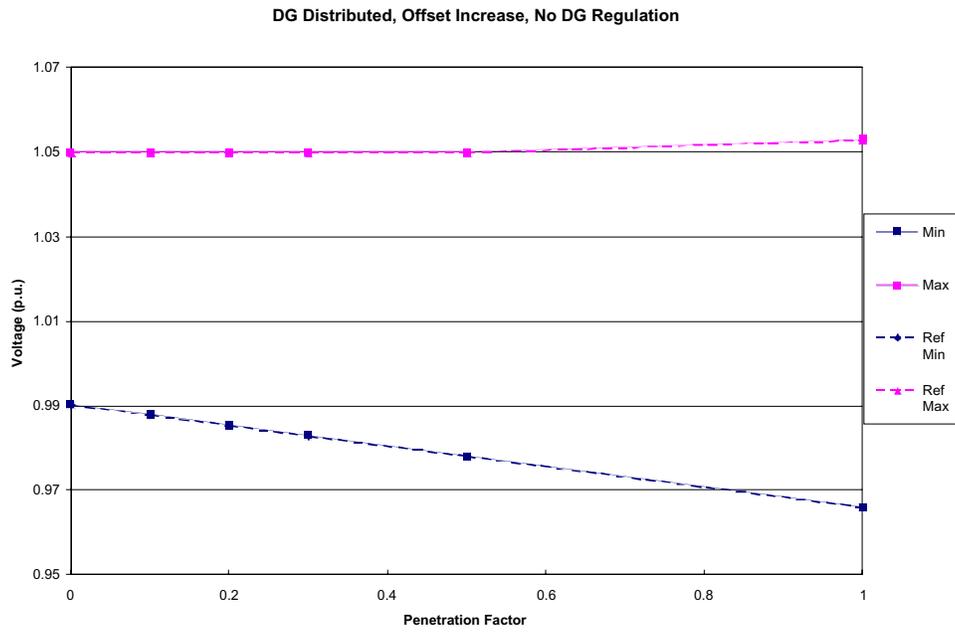
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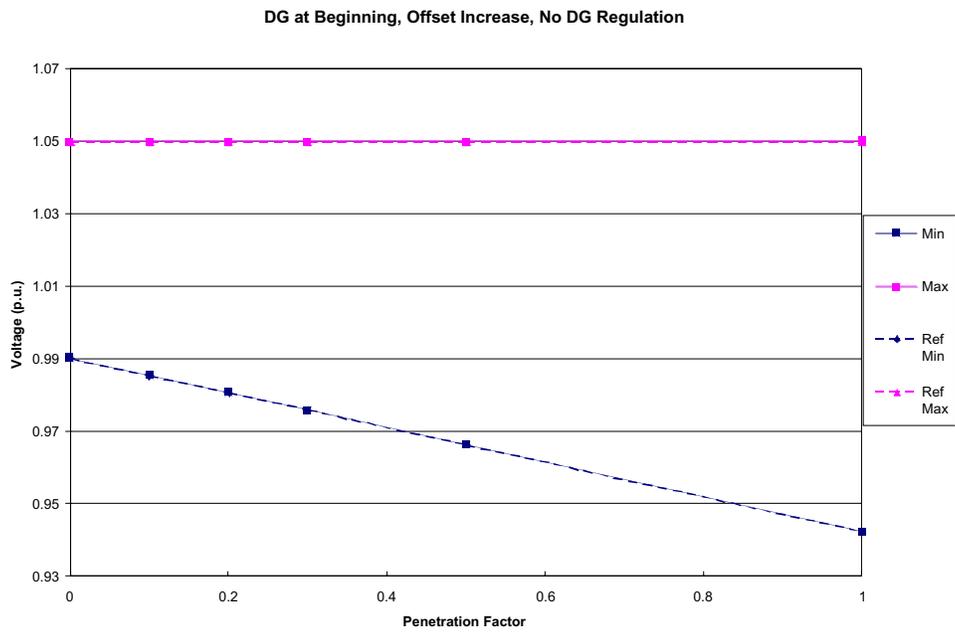
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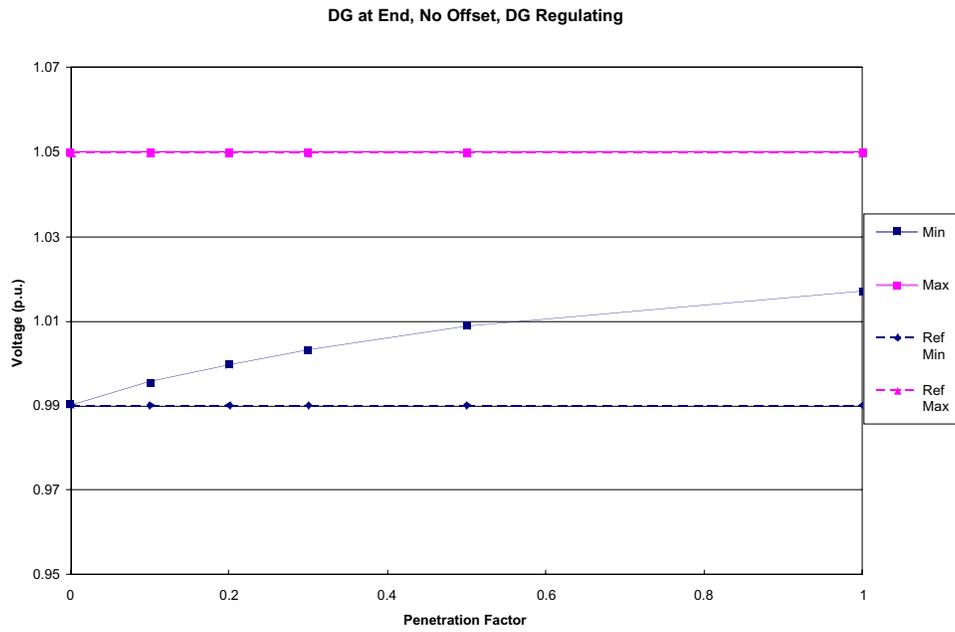
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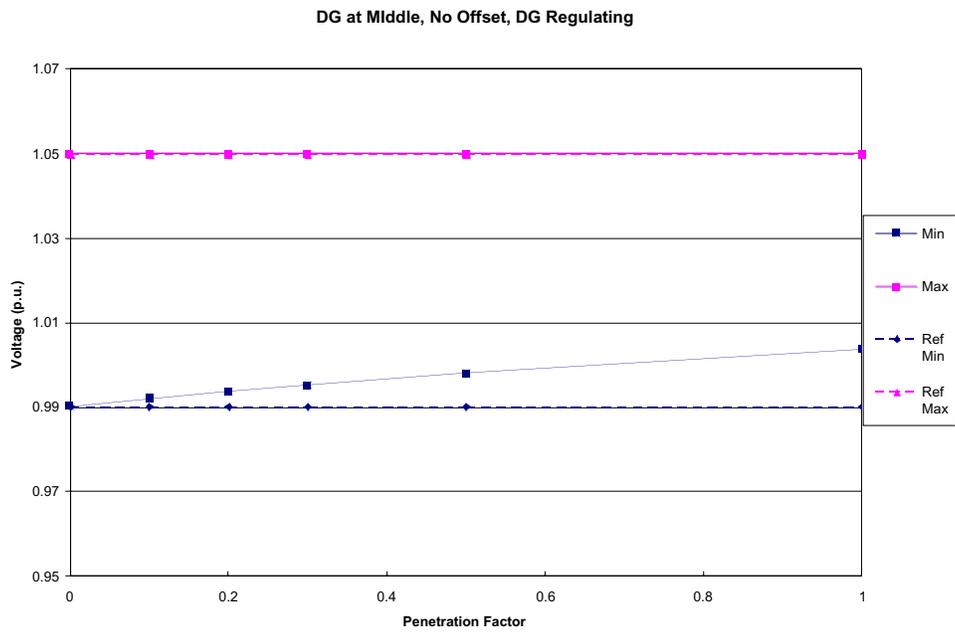
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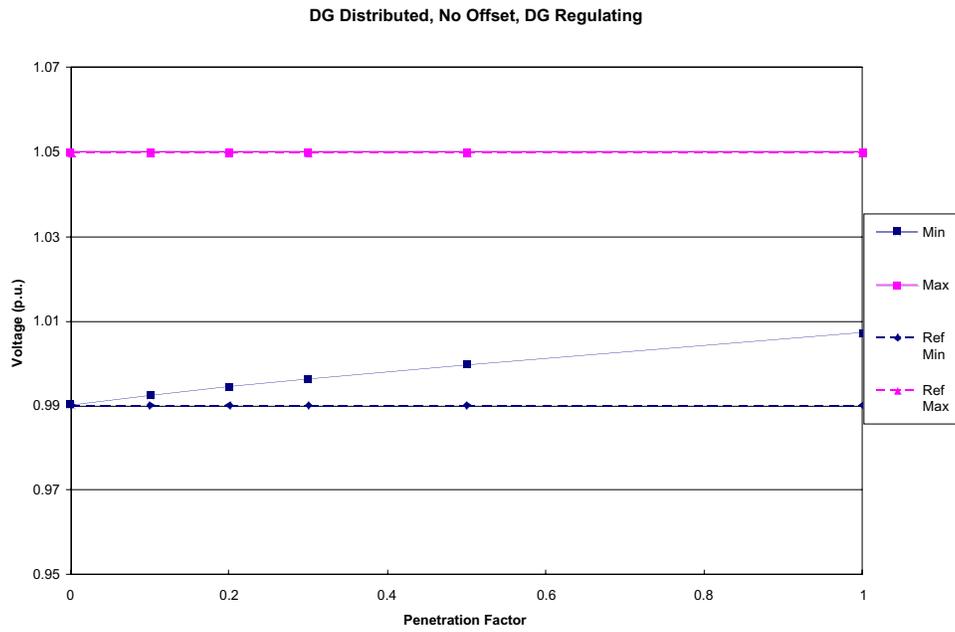
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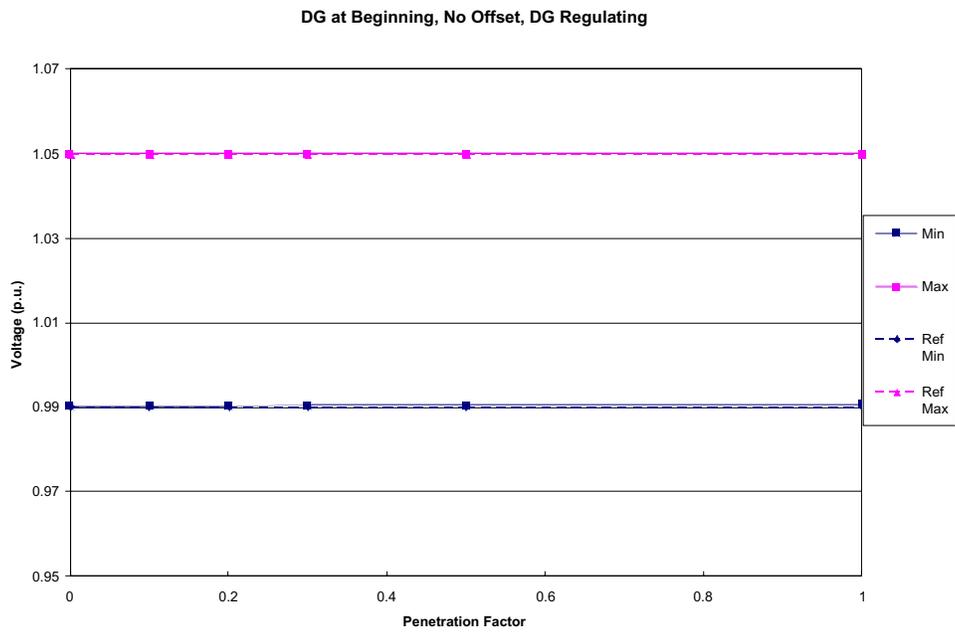
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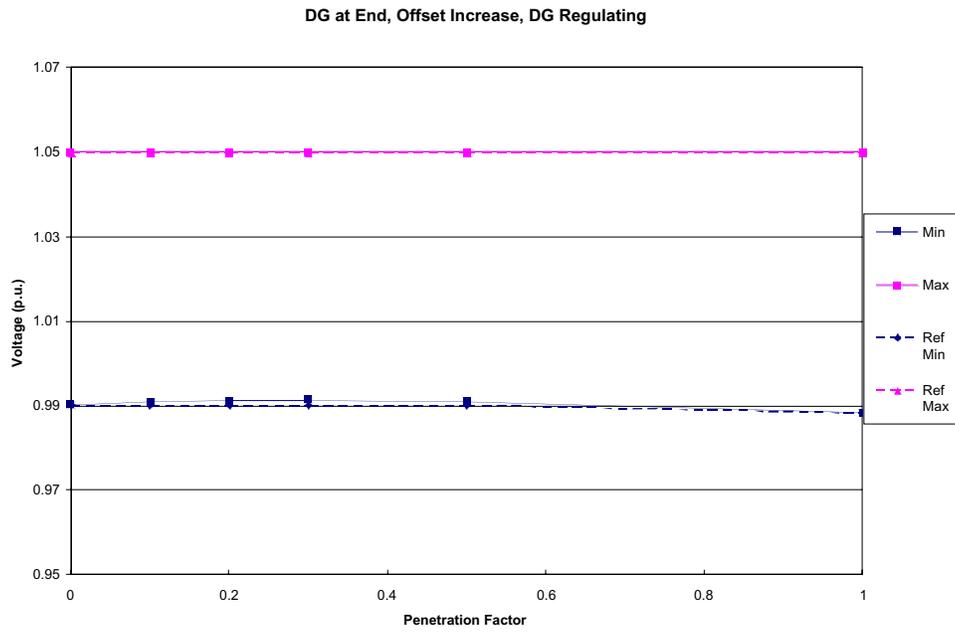
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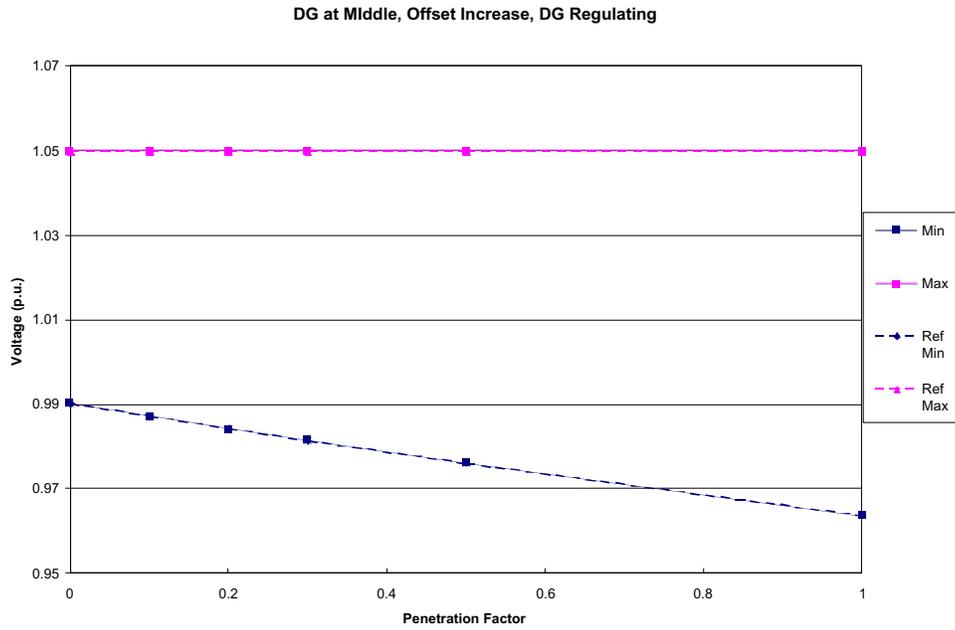
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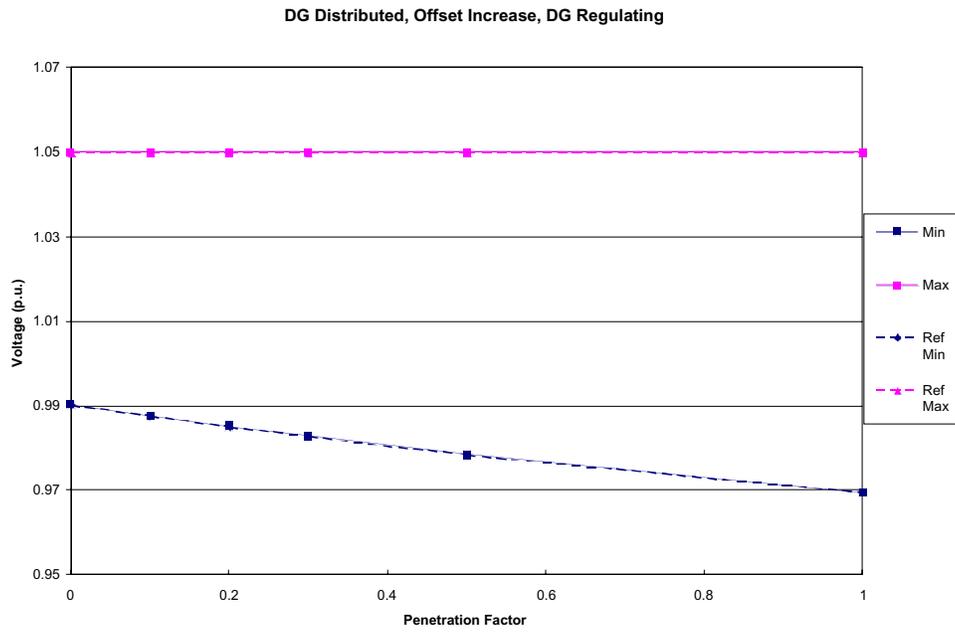
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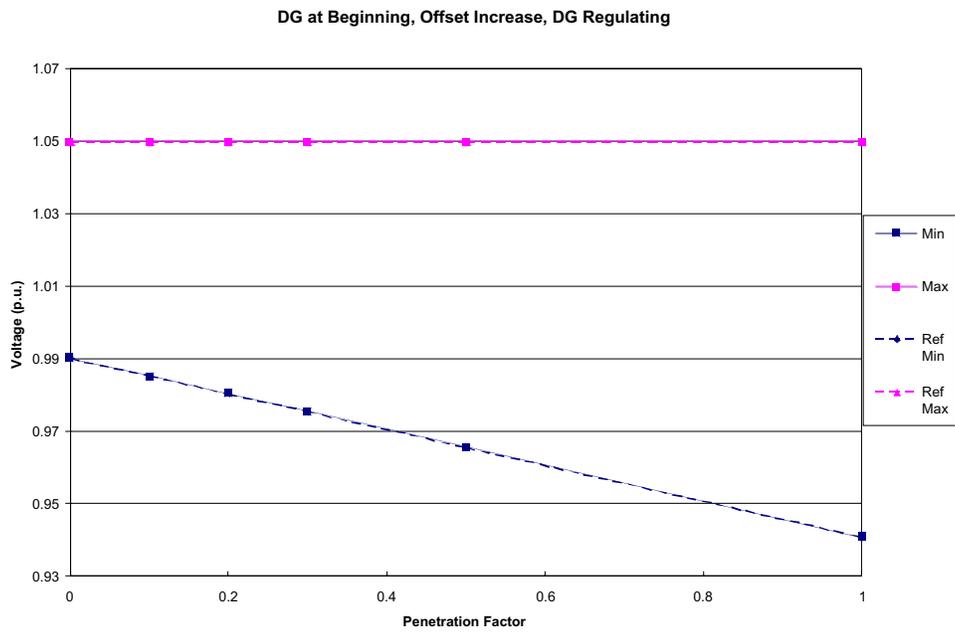
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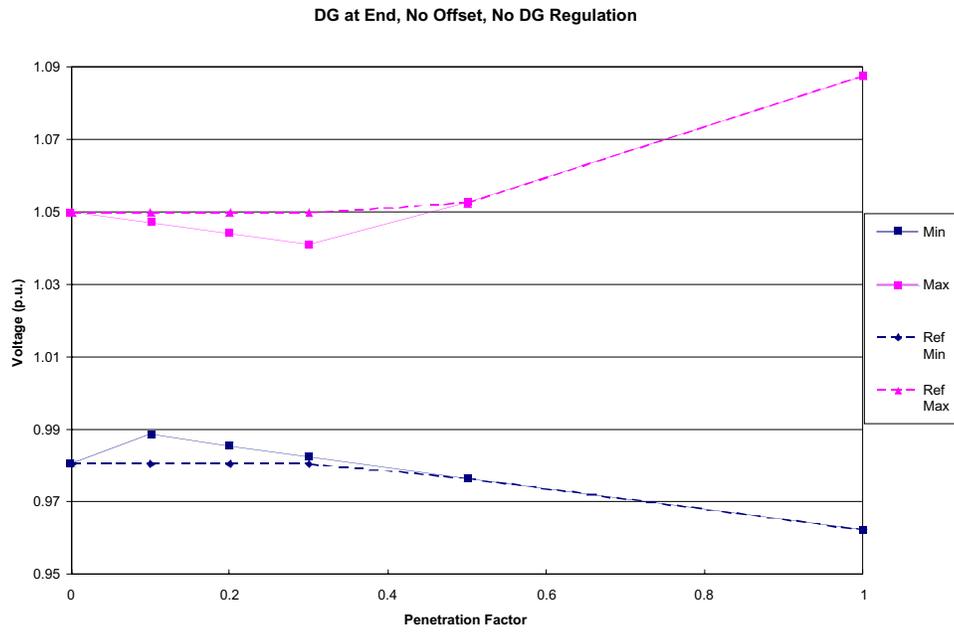


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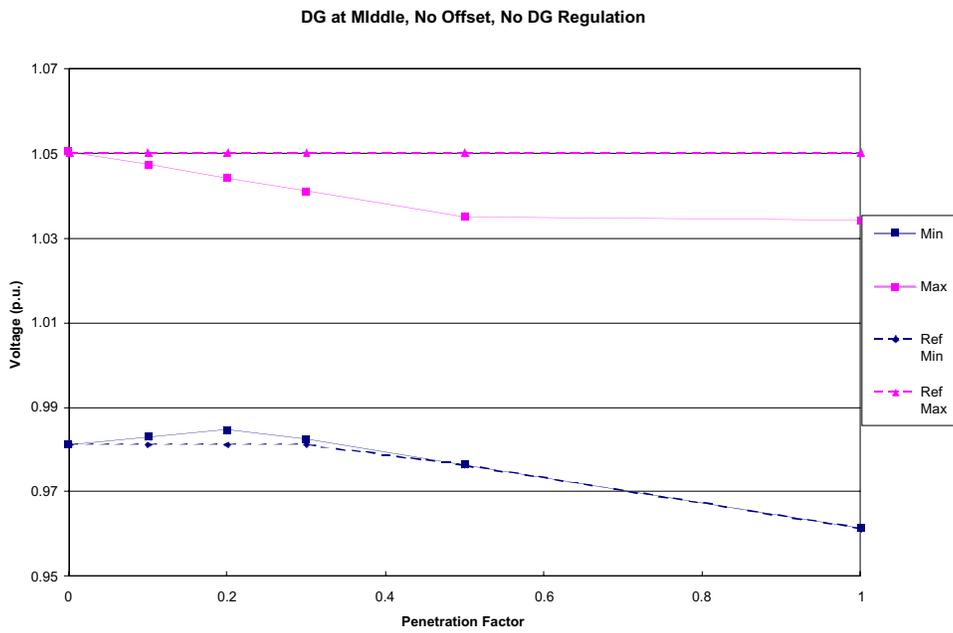


## BASE DESIGN 2.1

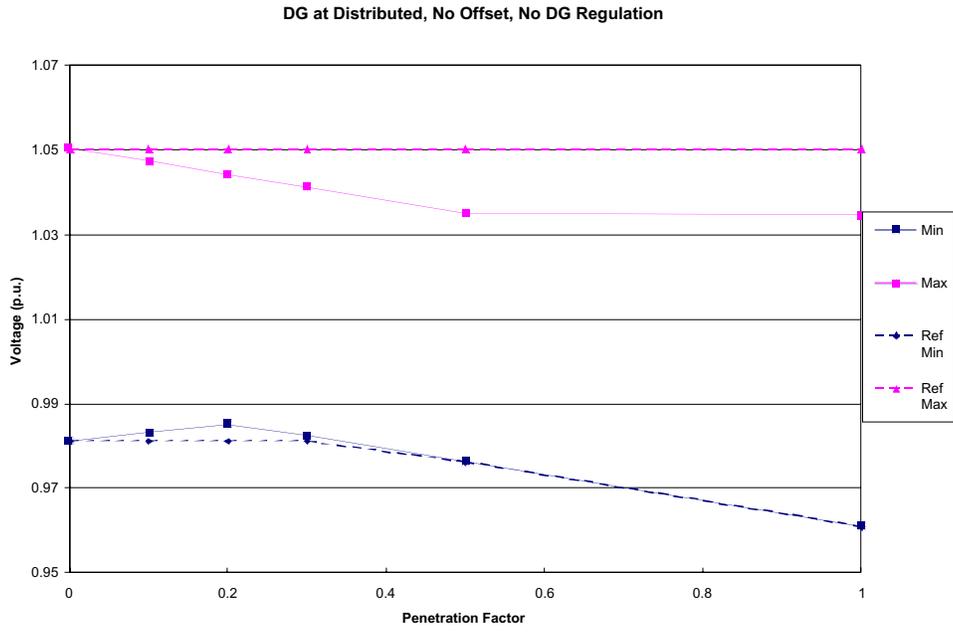
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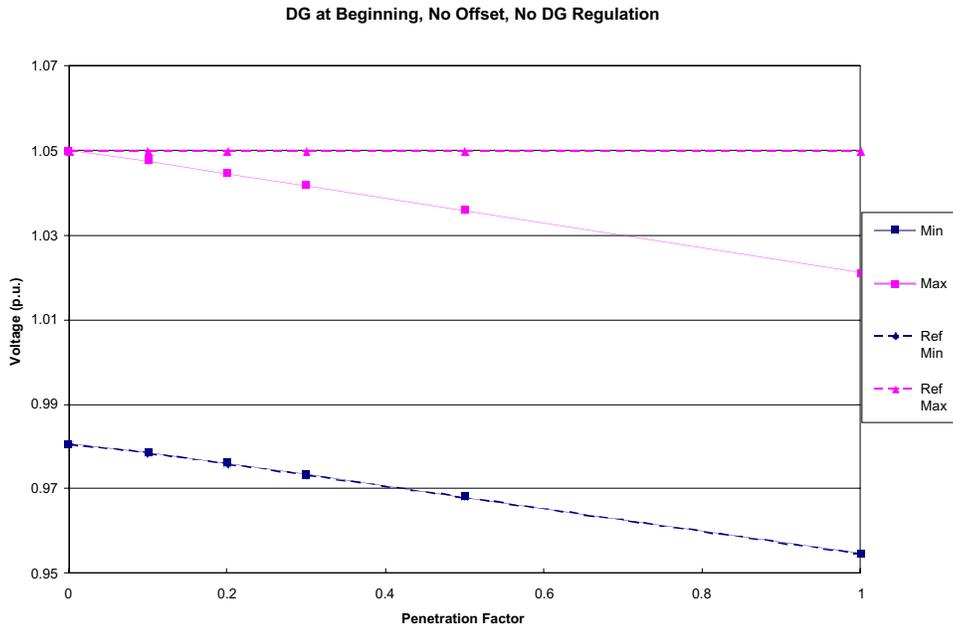
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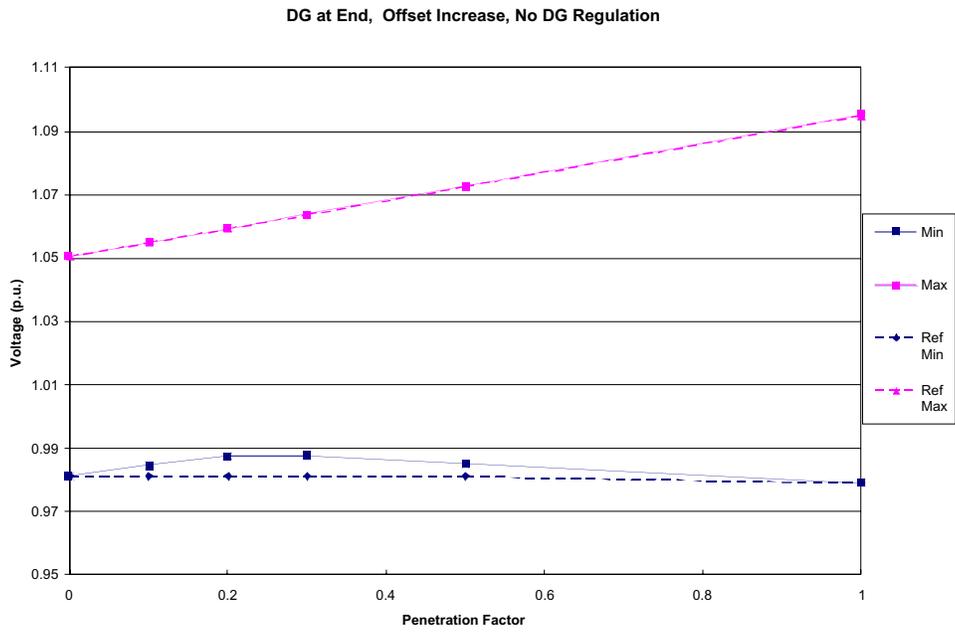
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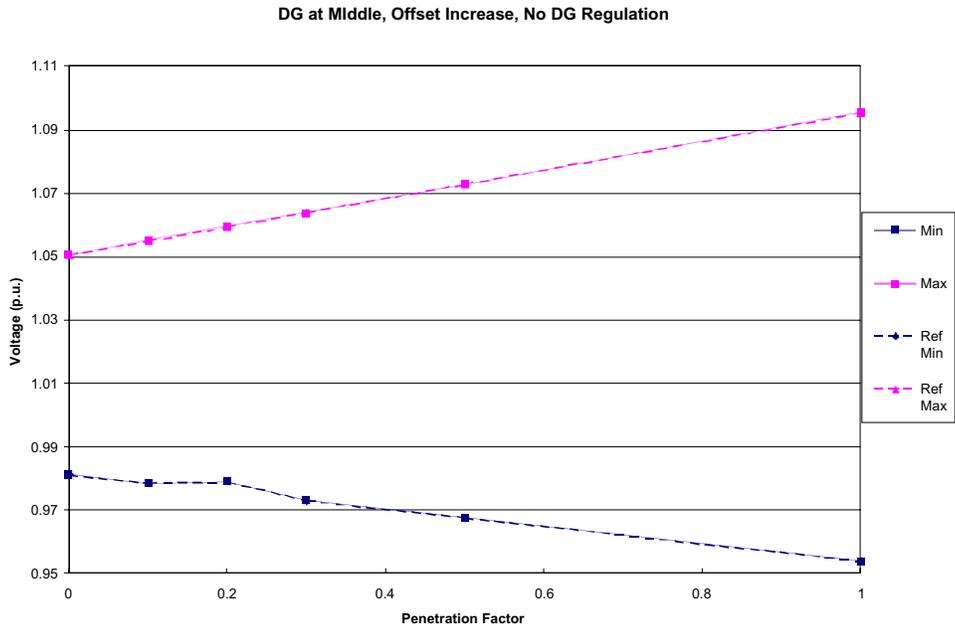
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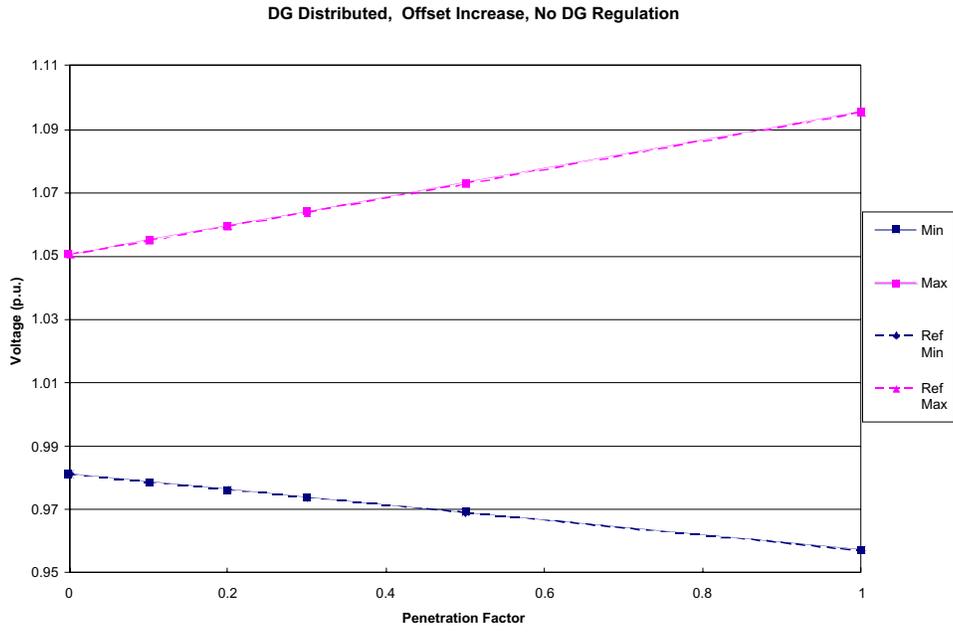
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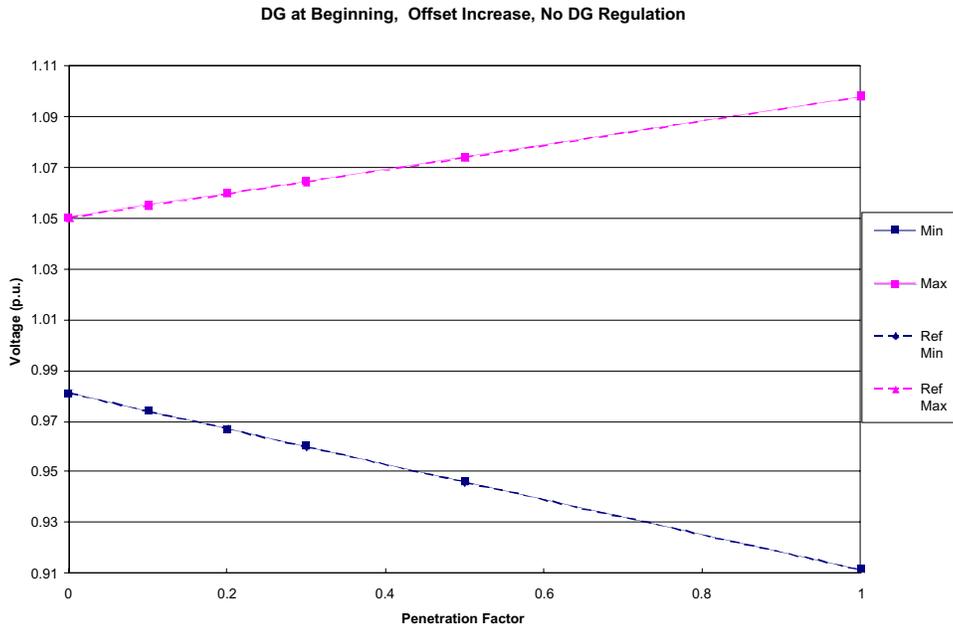
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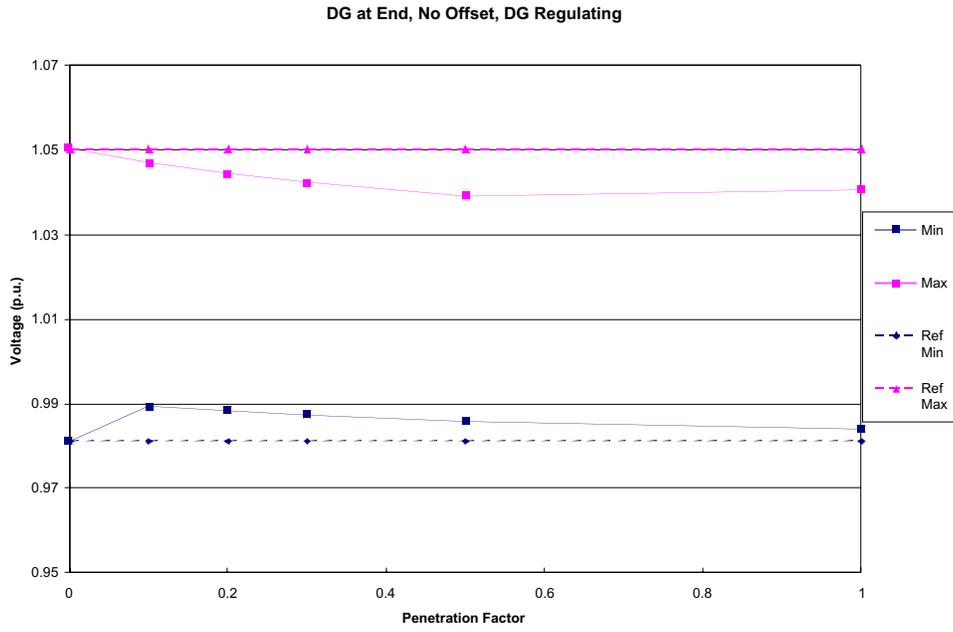
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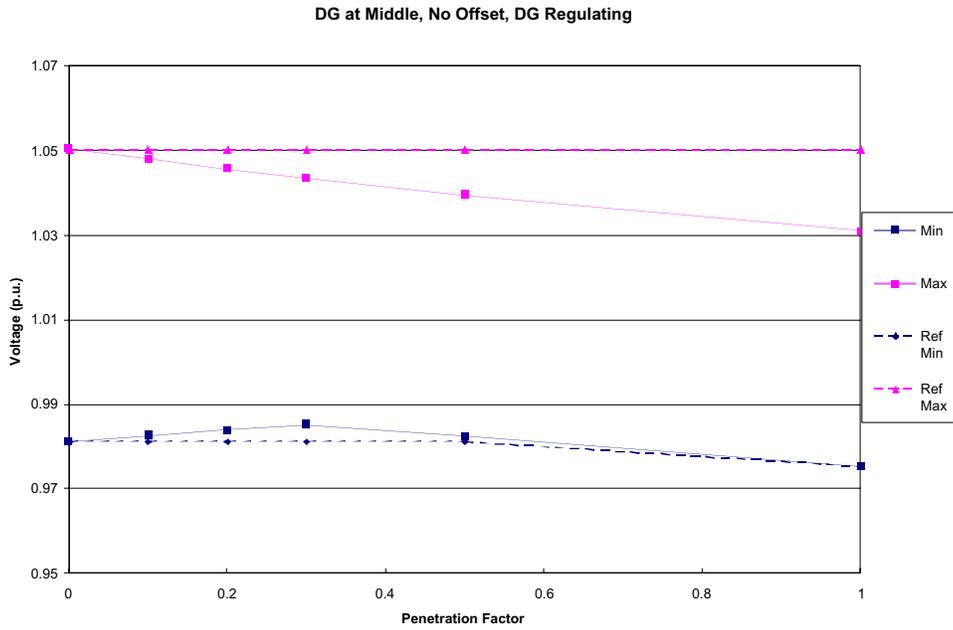
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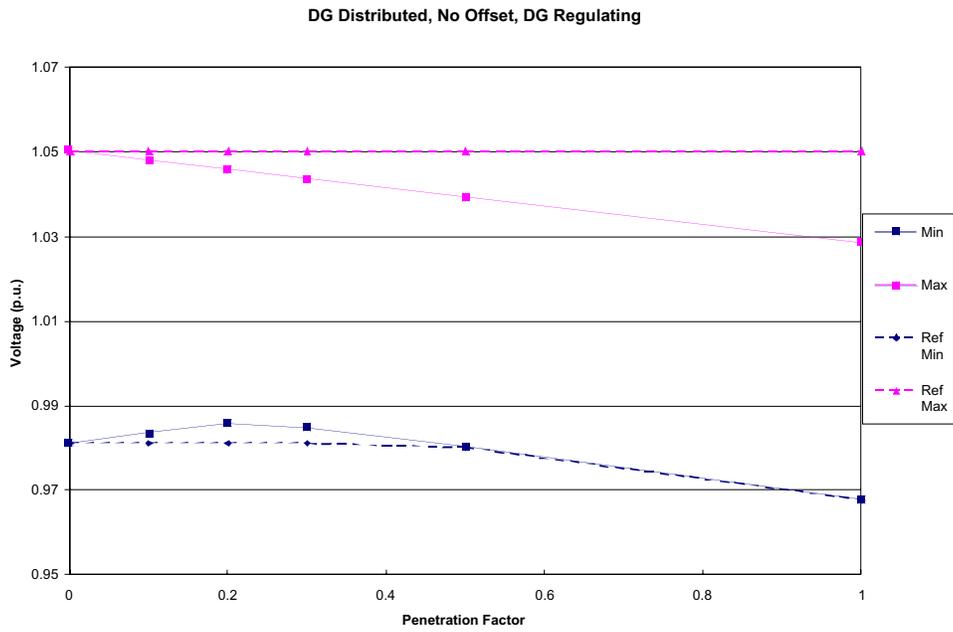
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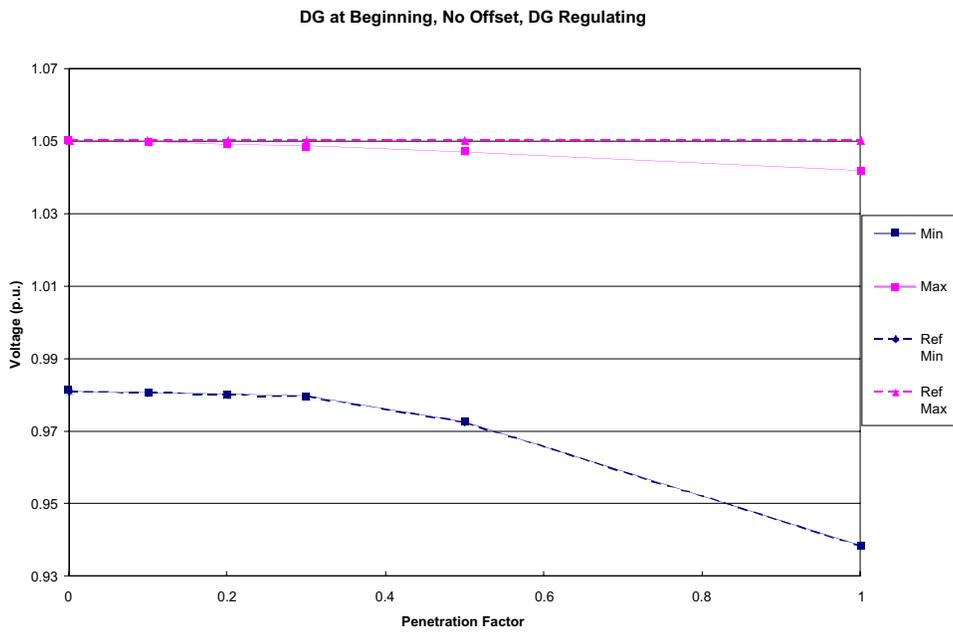
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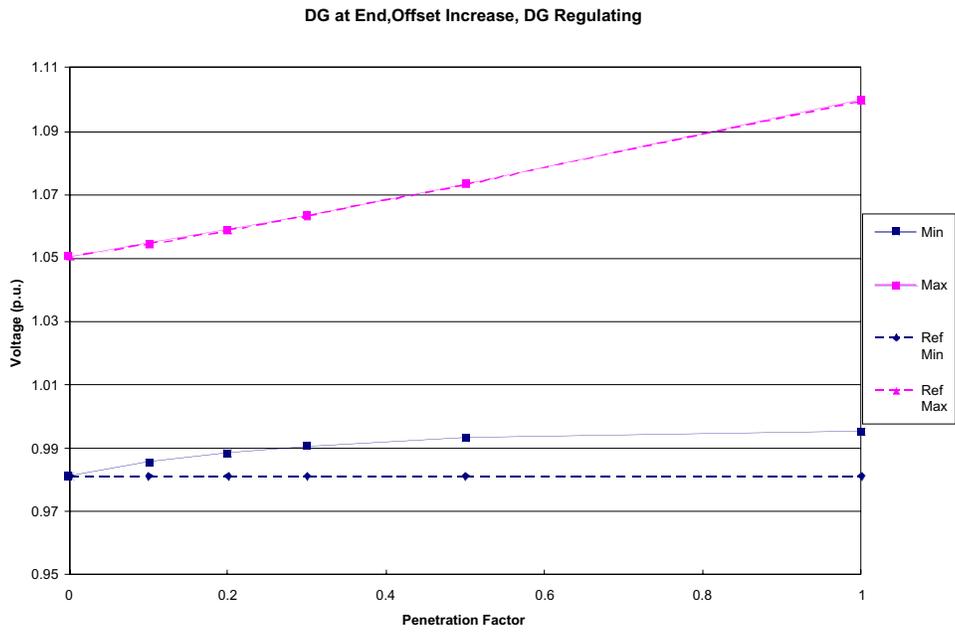
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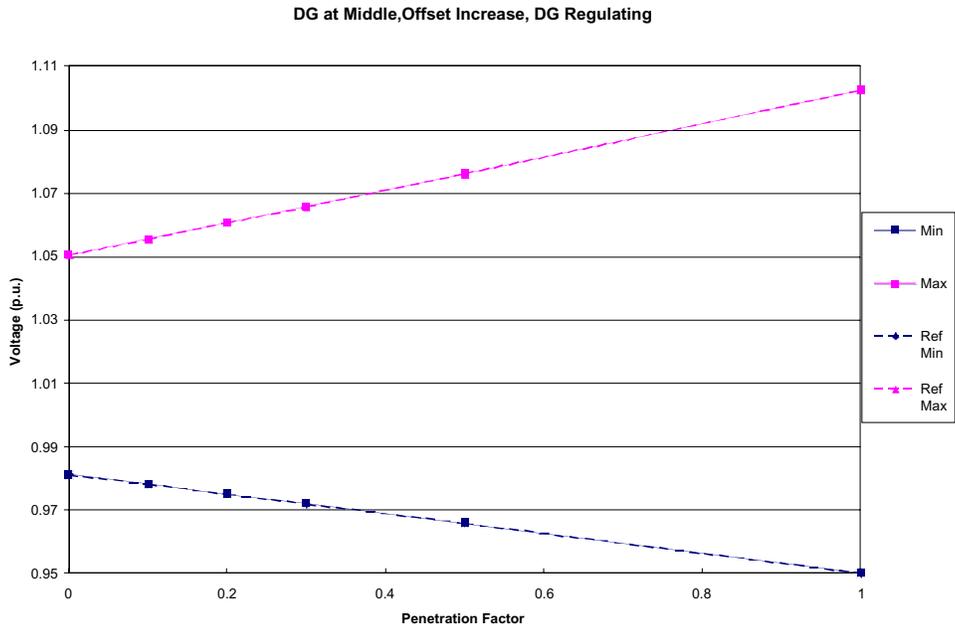
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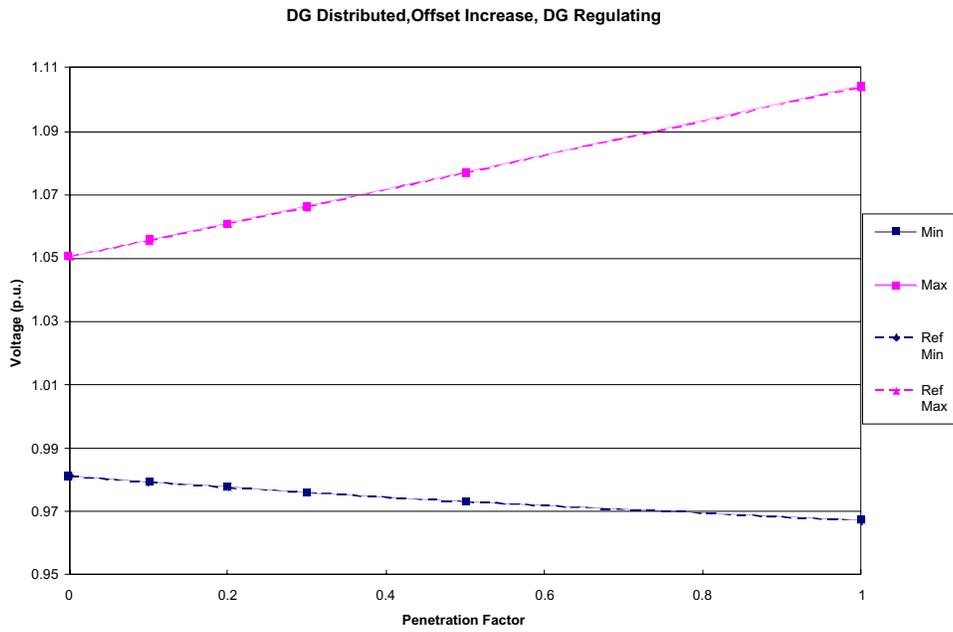
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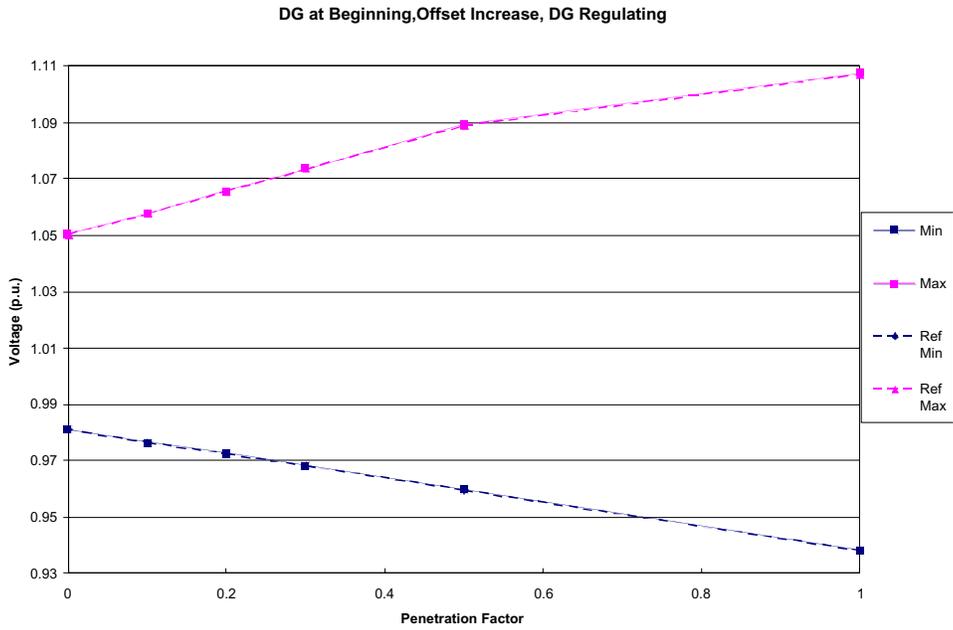
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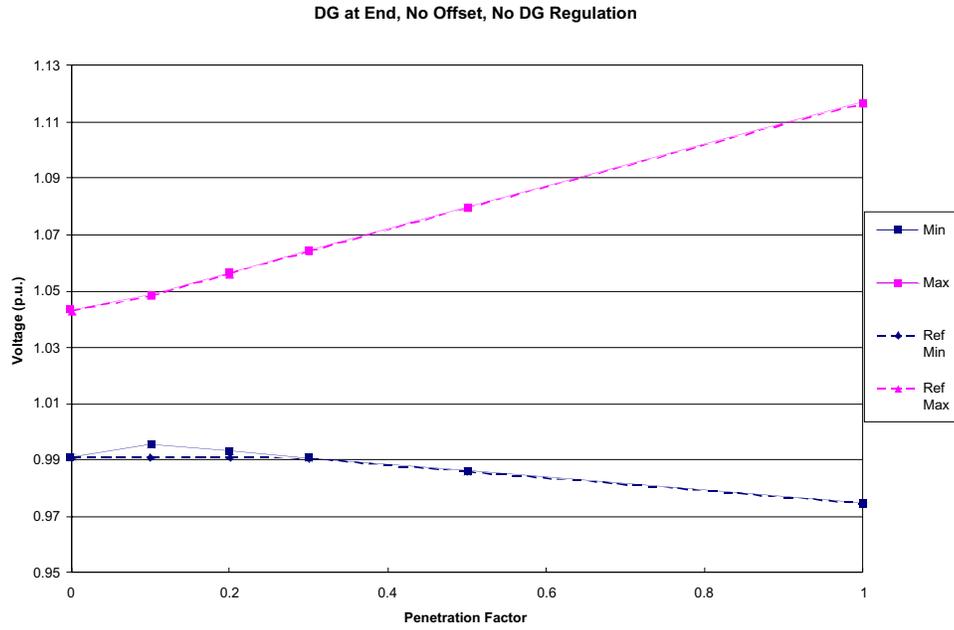


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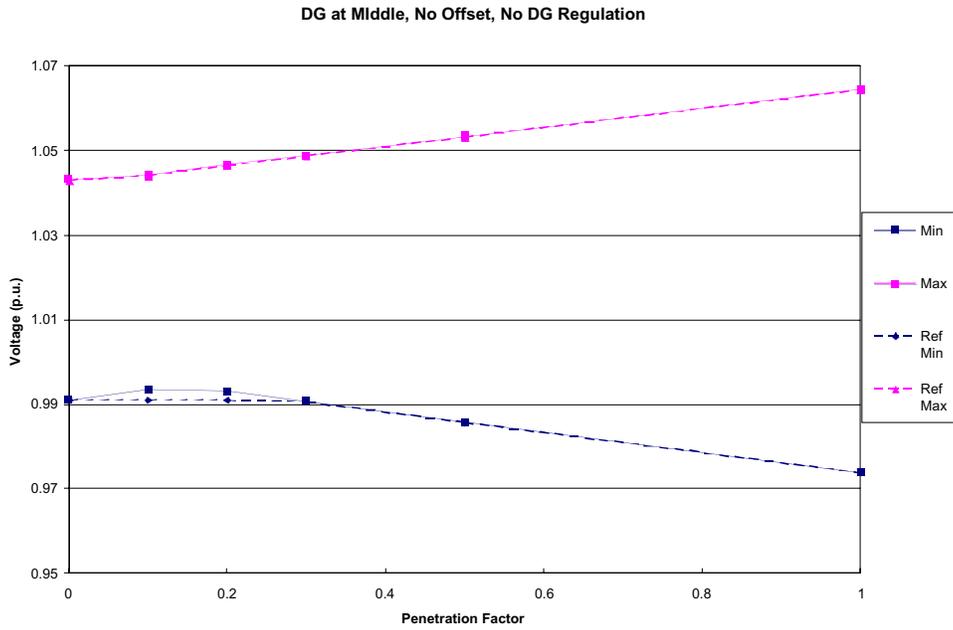


## BASE DESIGN 2.2

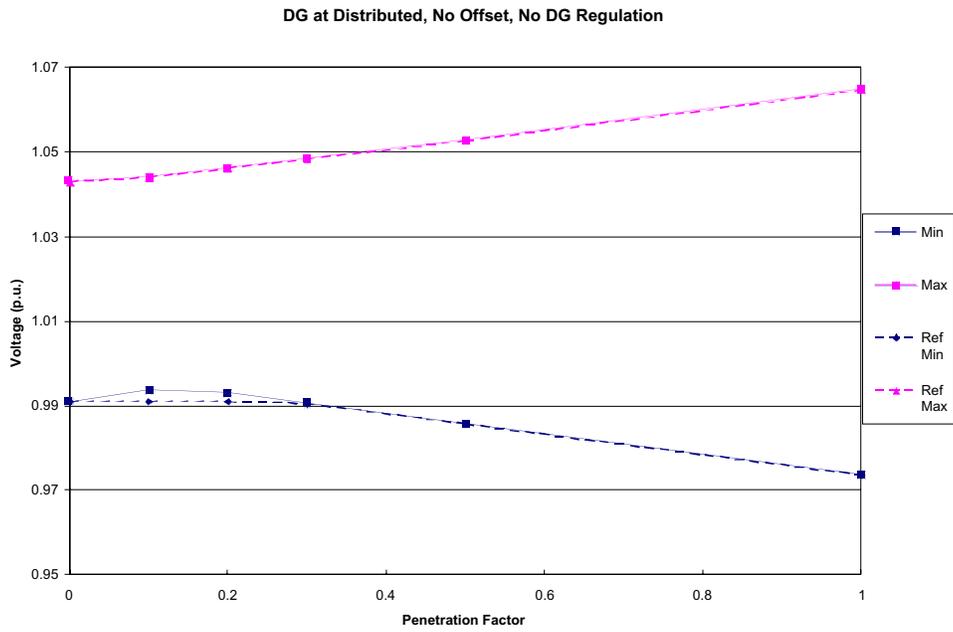
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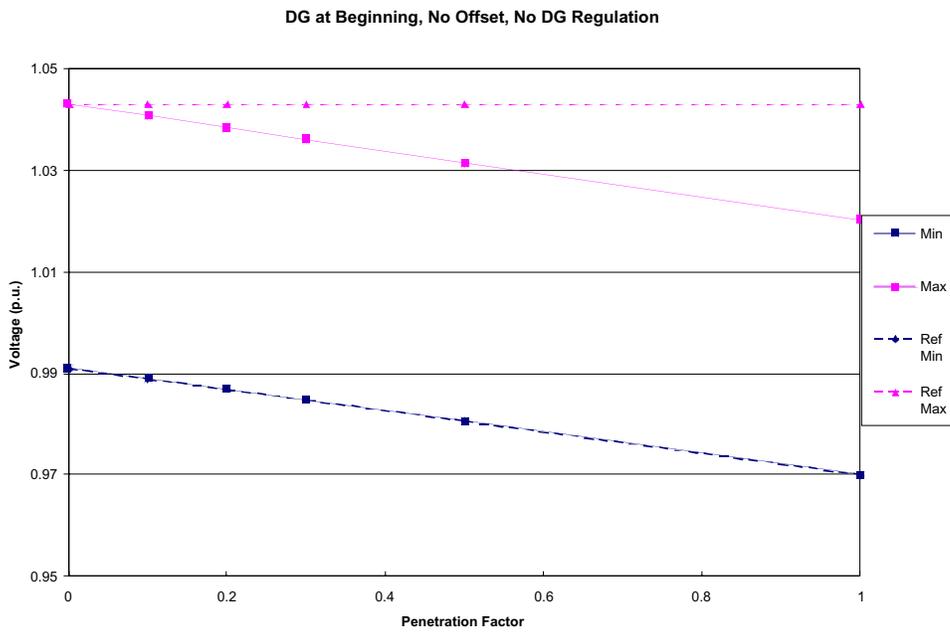
### 2.2.1.1.2



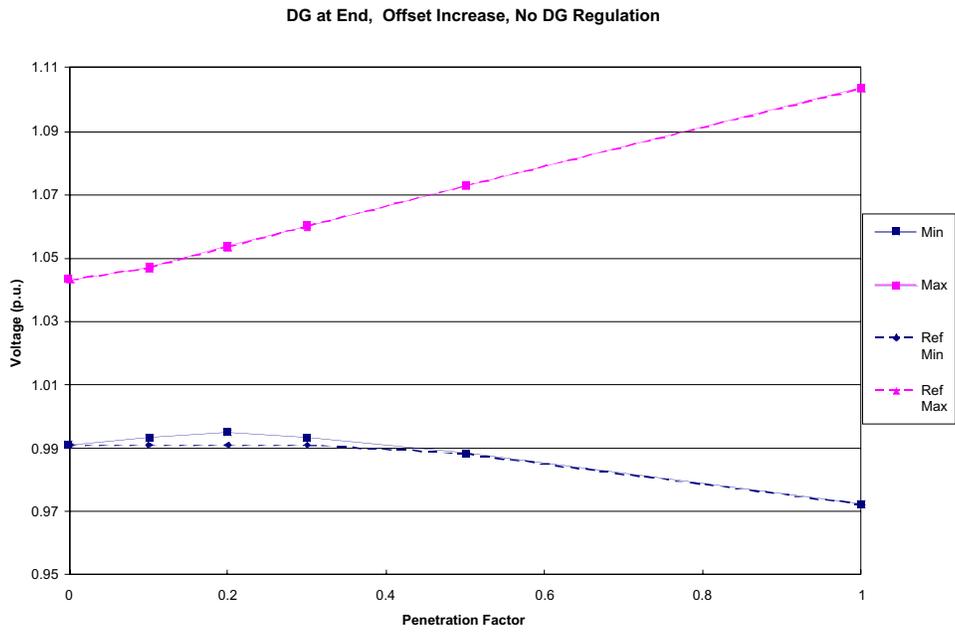
### 2.2.1.1.3



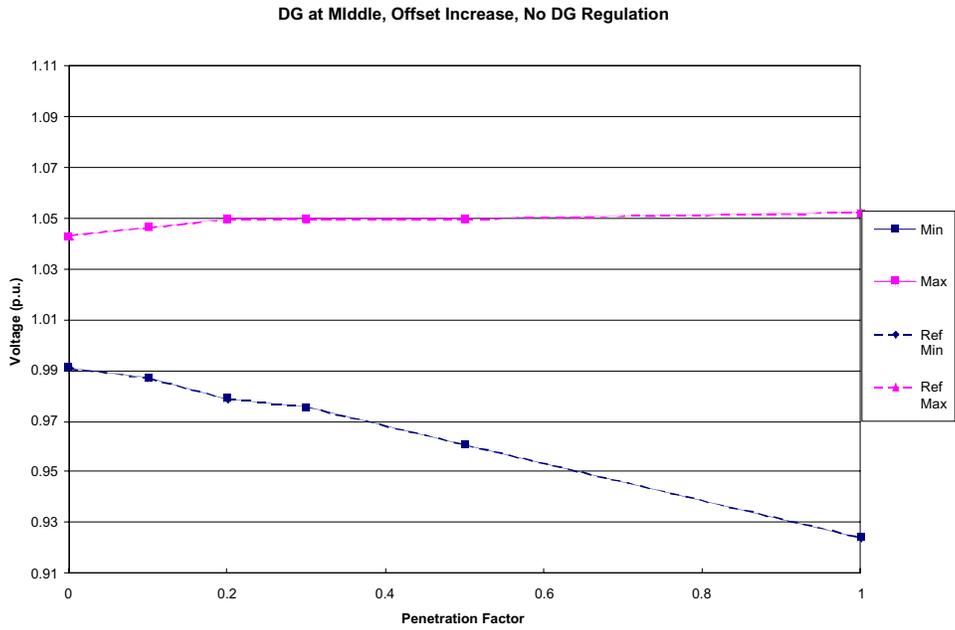
### 2.2.1.1.4



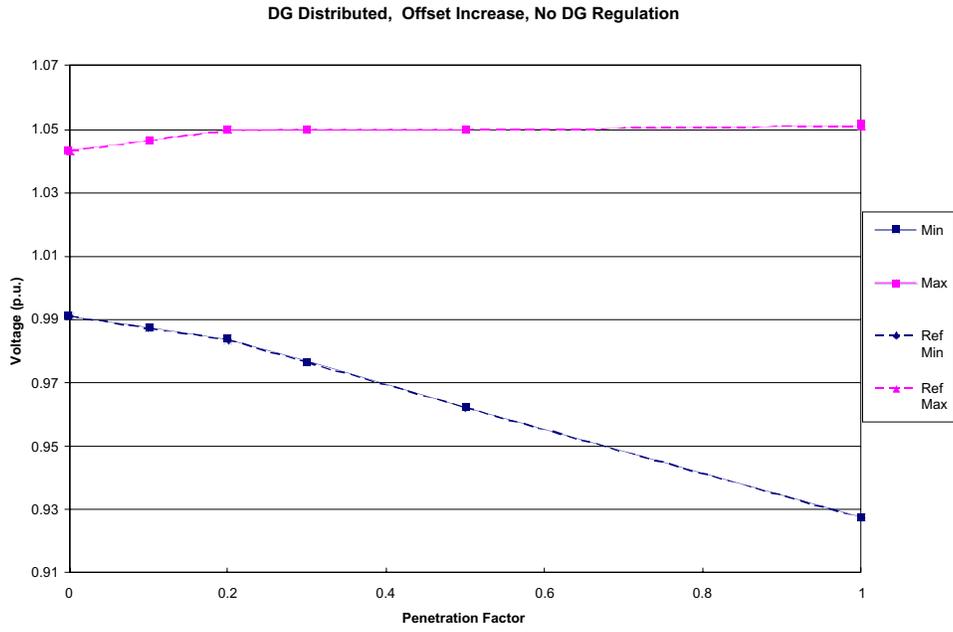
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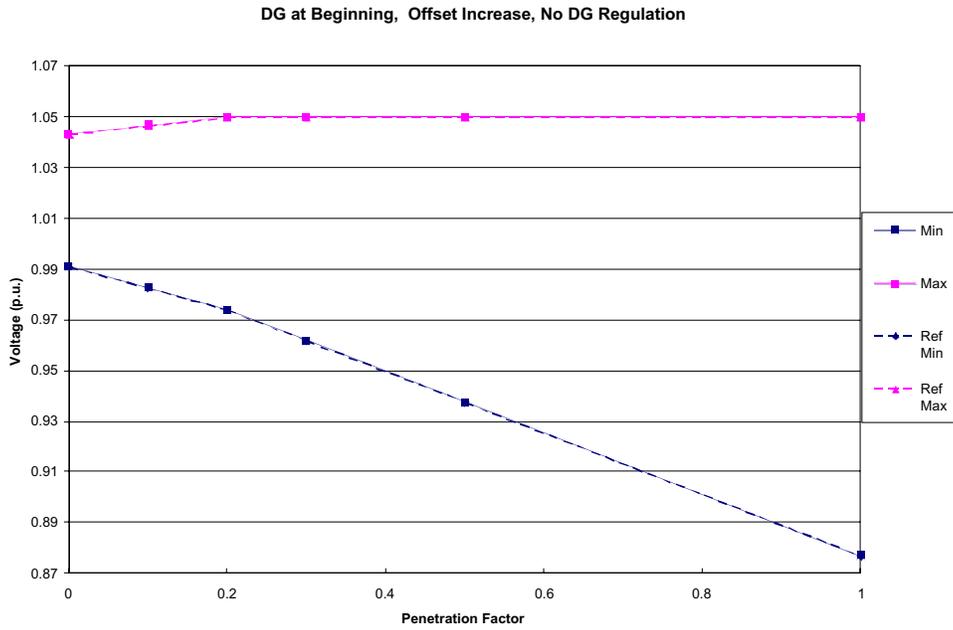
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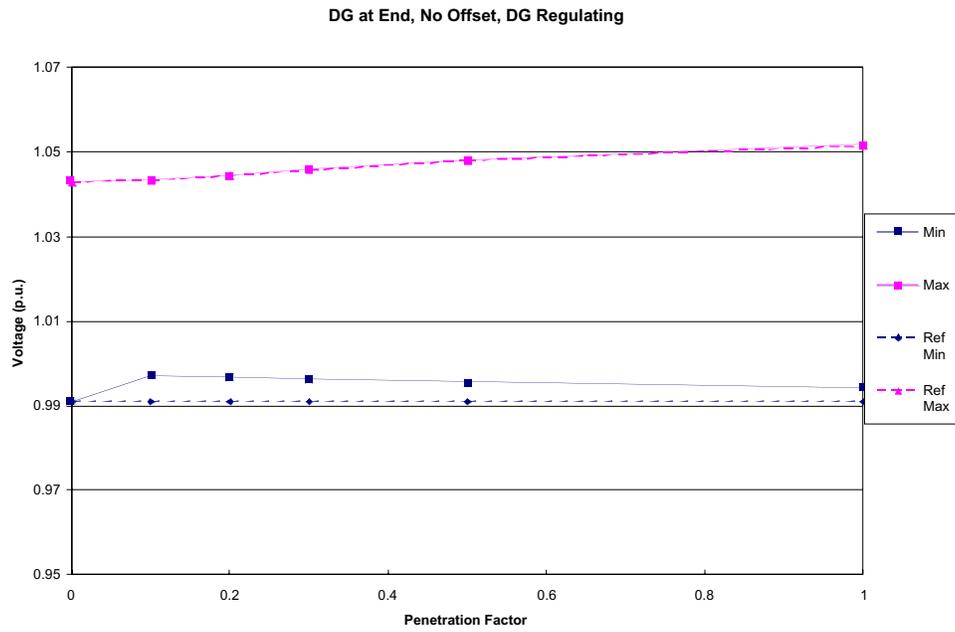
### 2.2.1.2.3



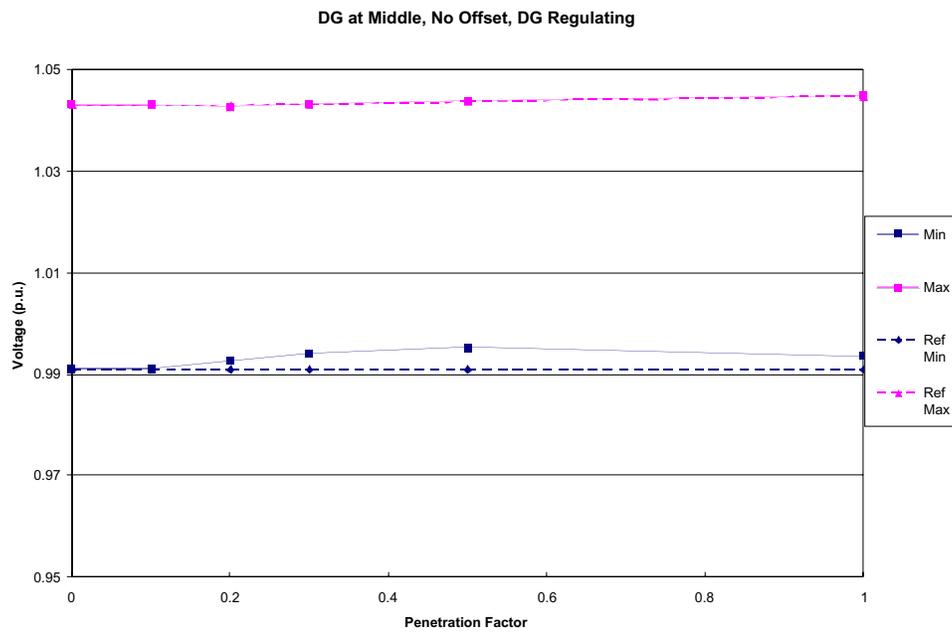
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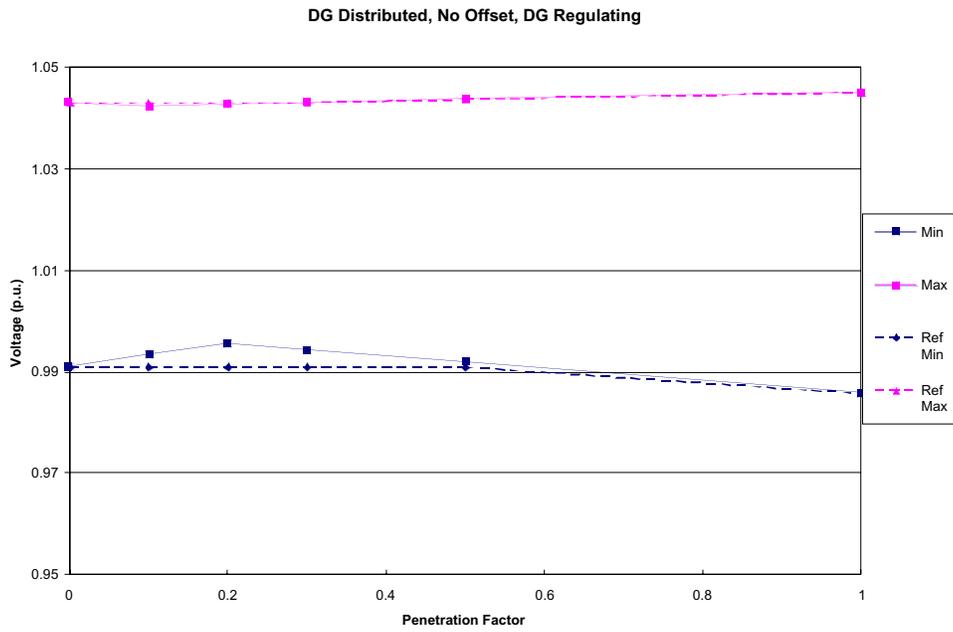
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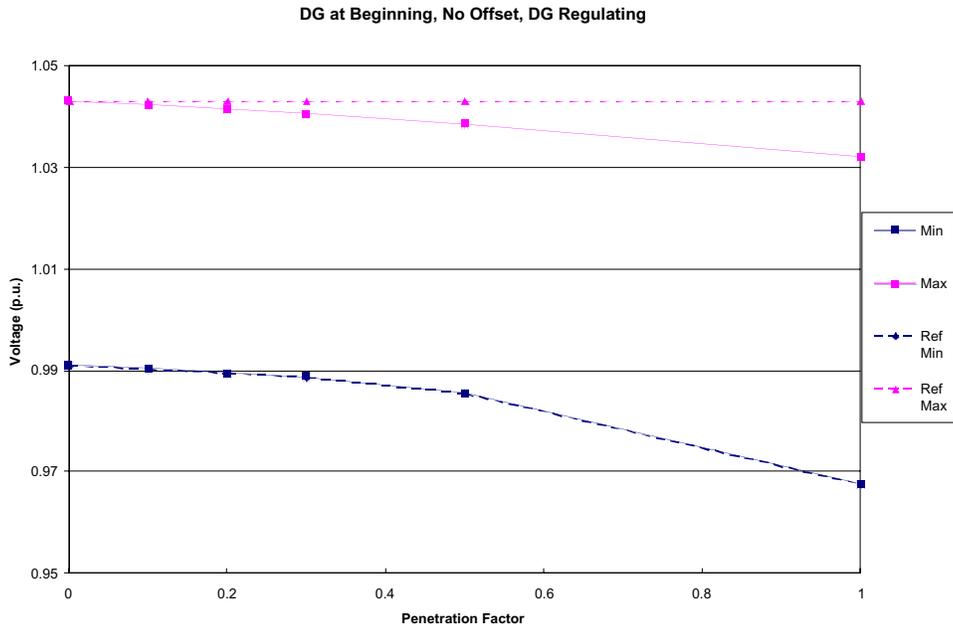
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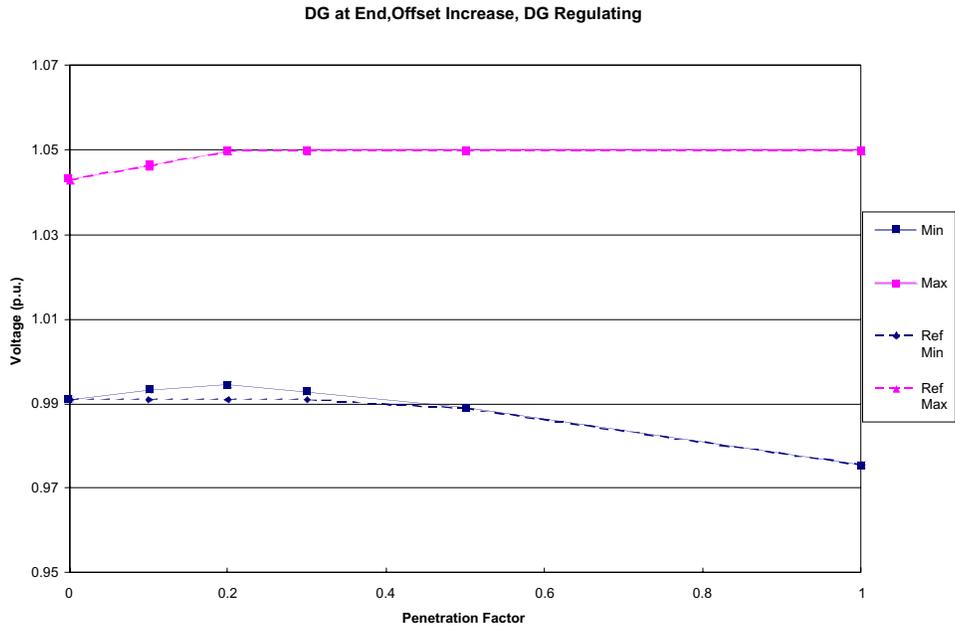
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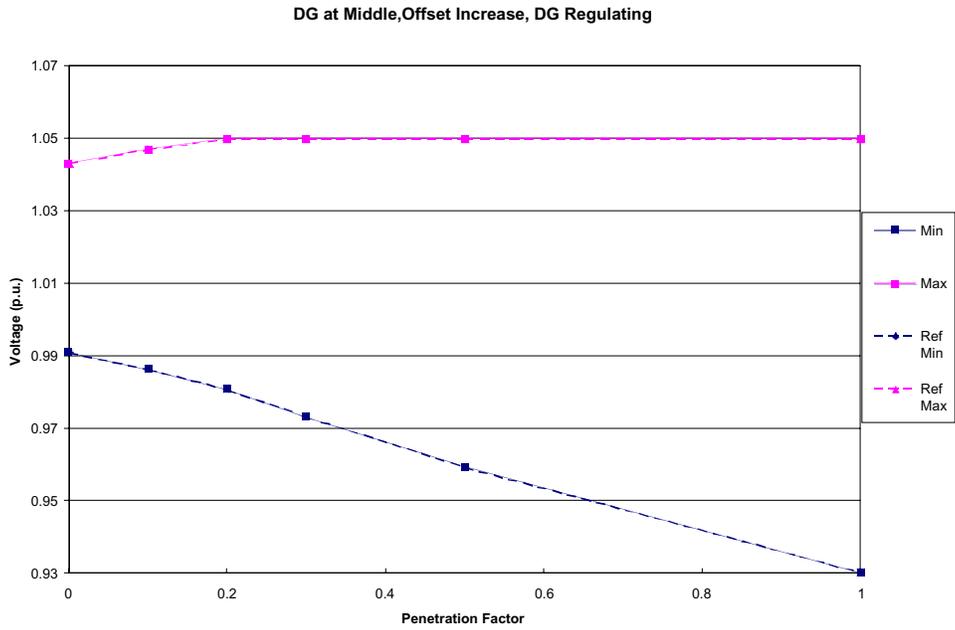
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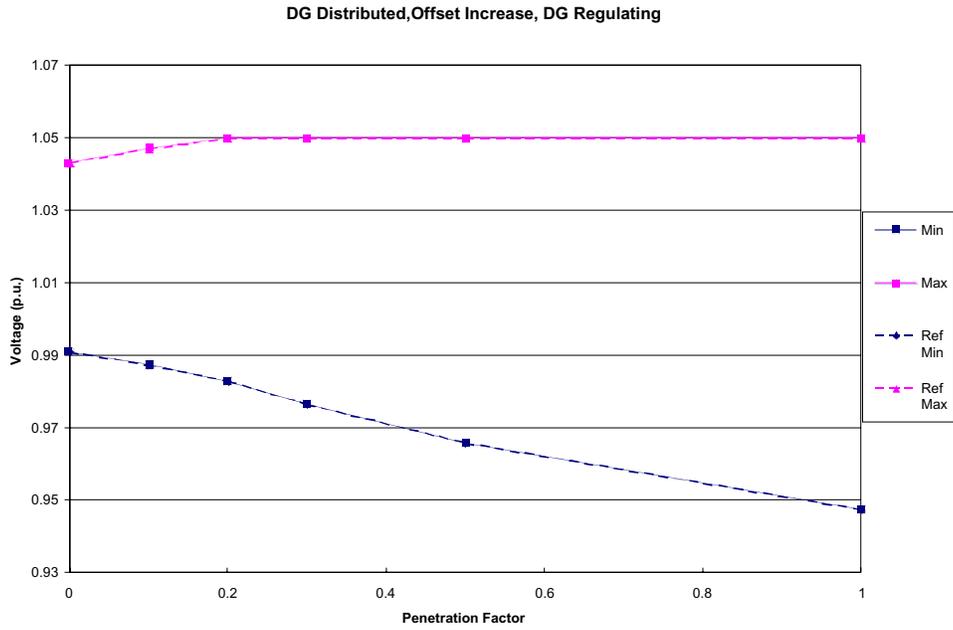
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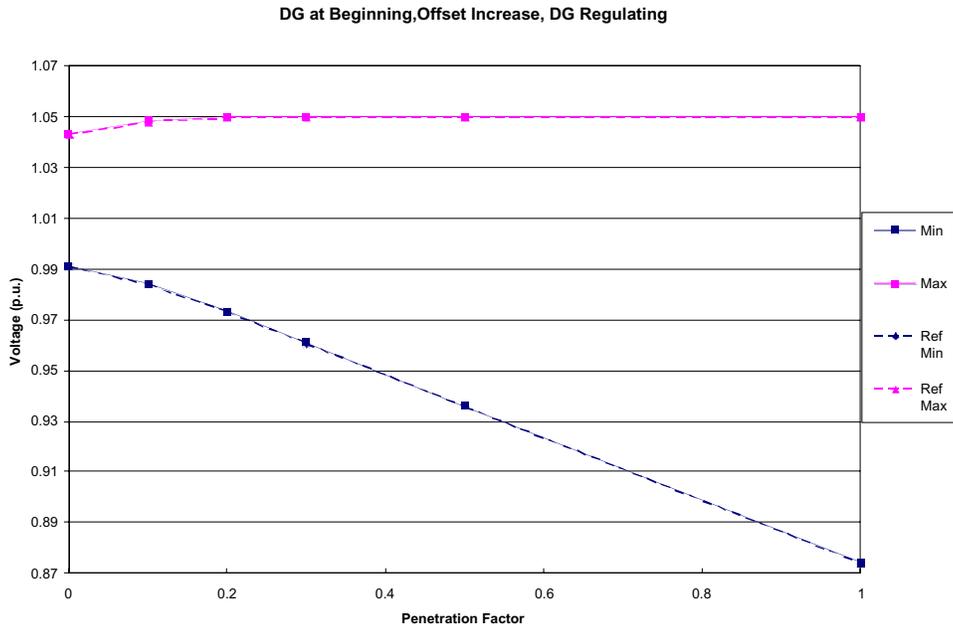
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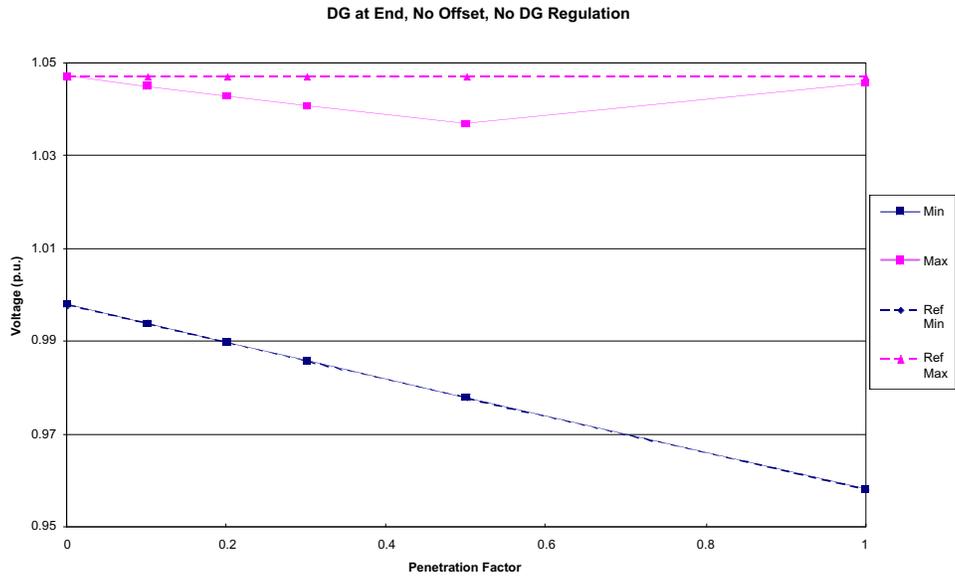


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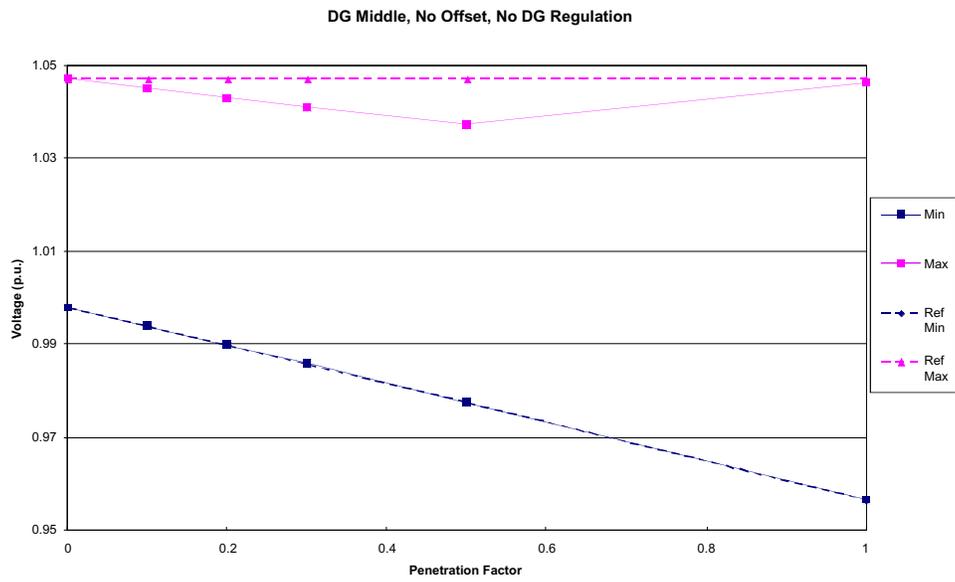


# BASE DESIGN 3.1

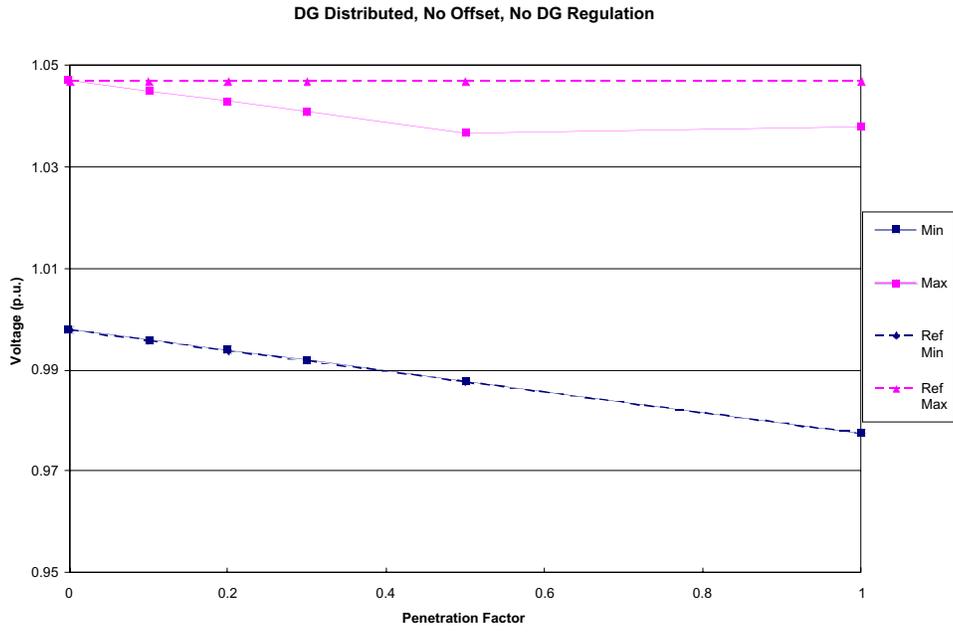
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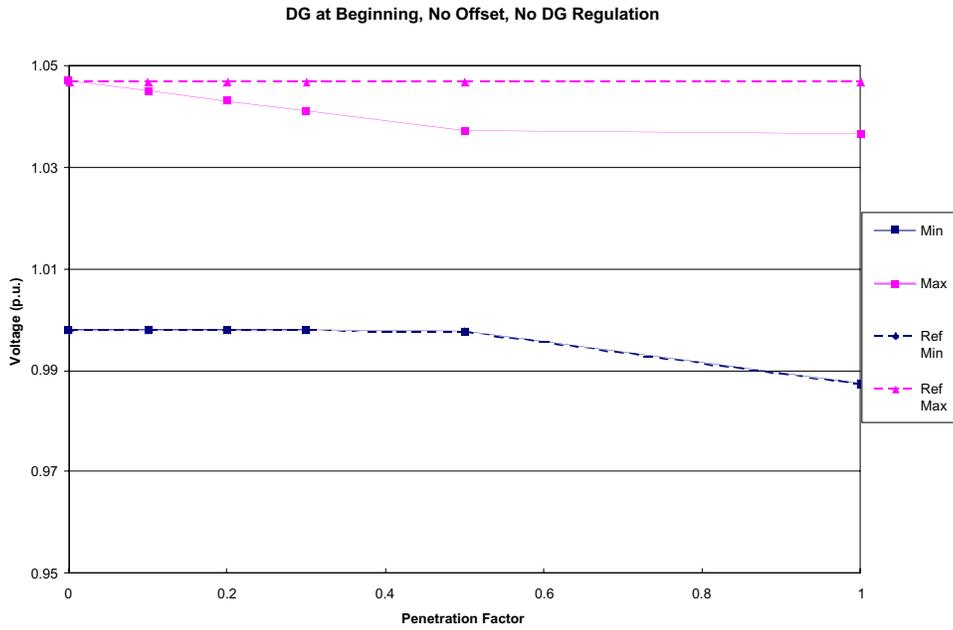
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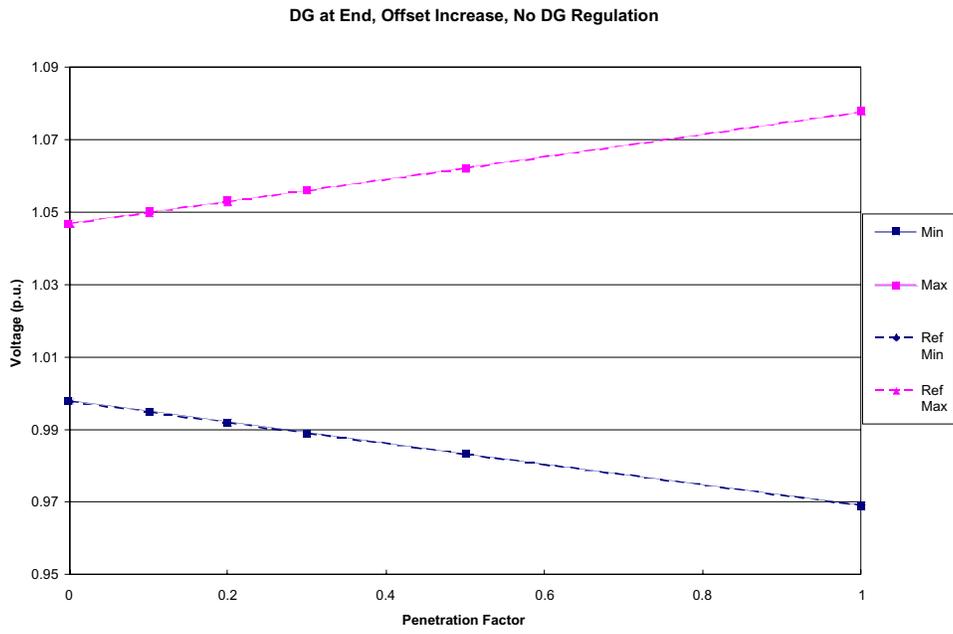
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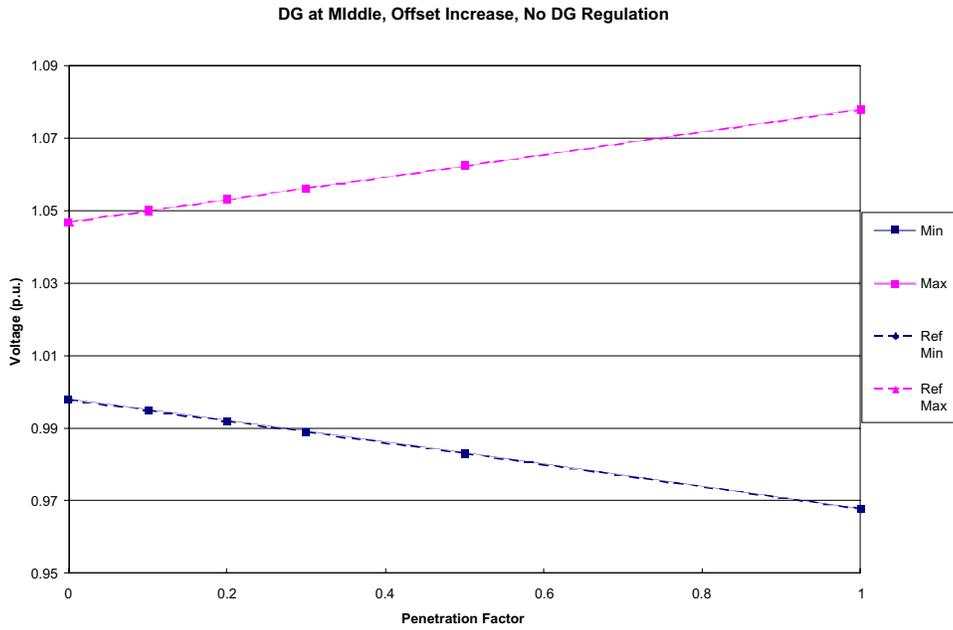
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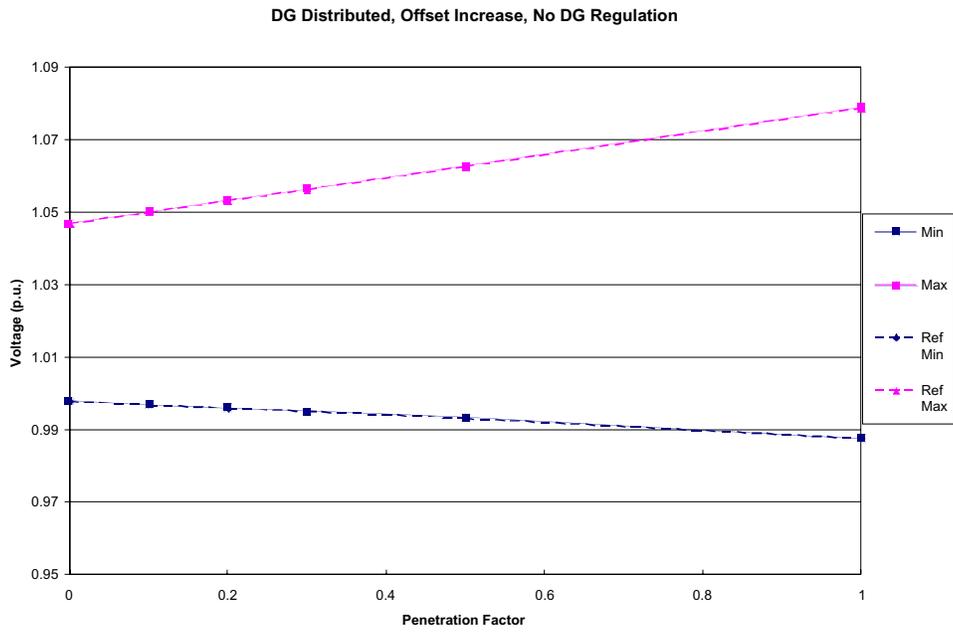
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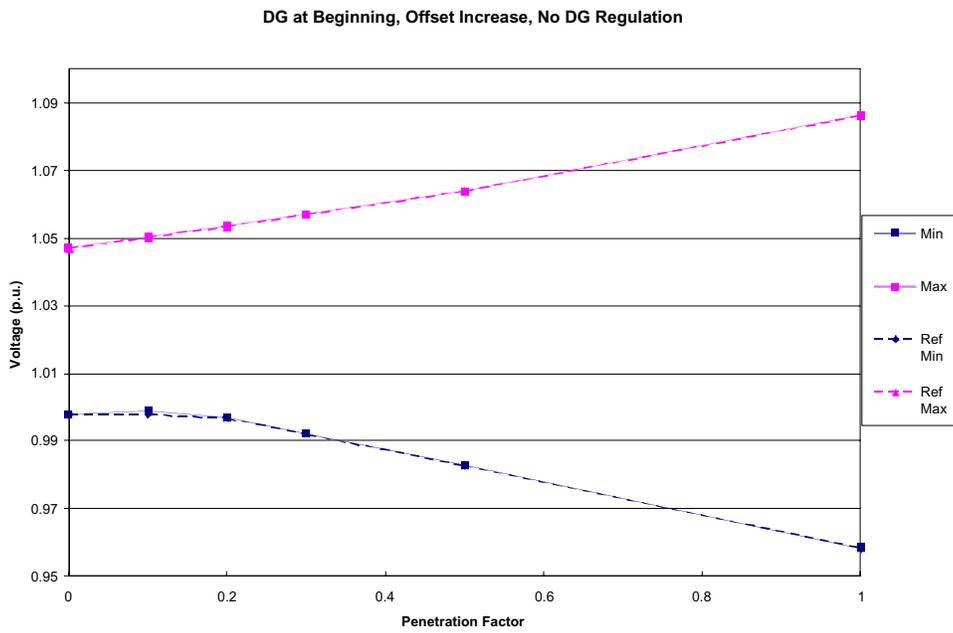
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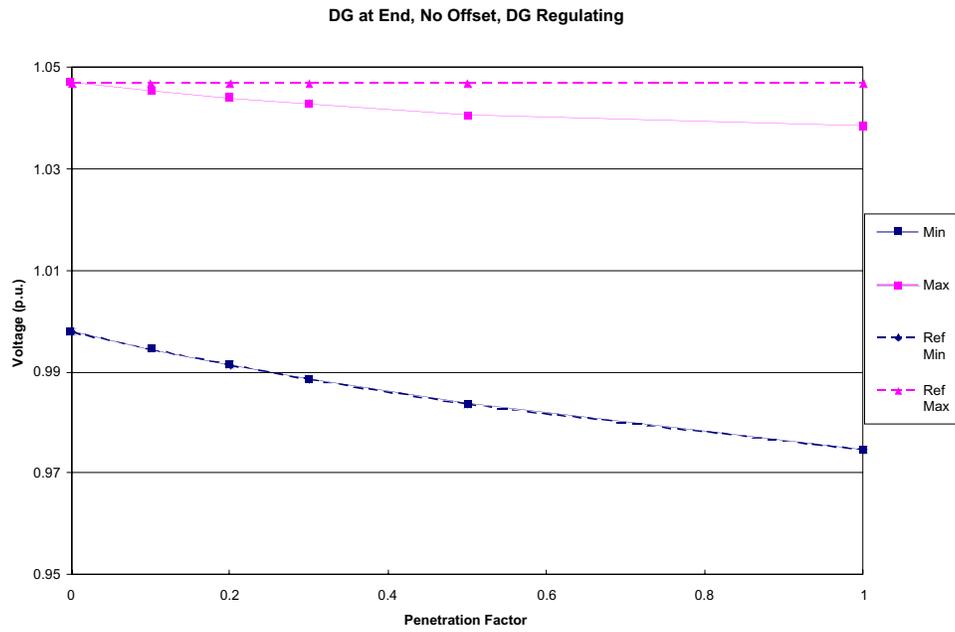
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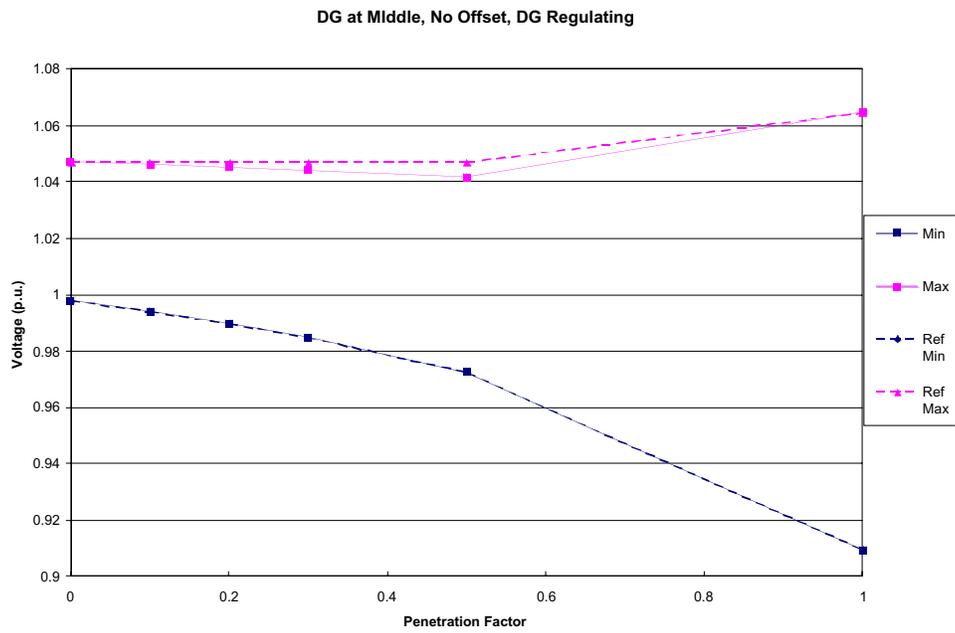
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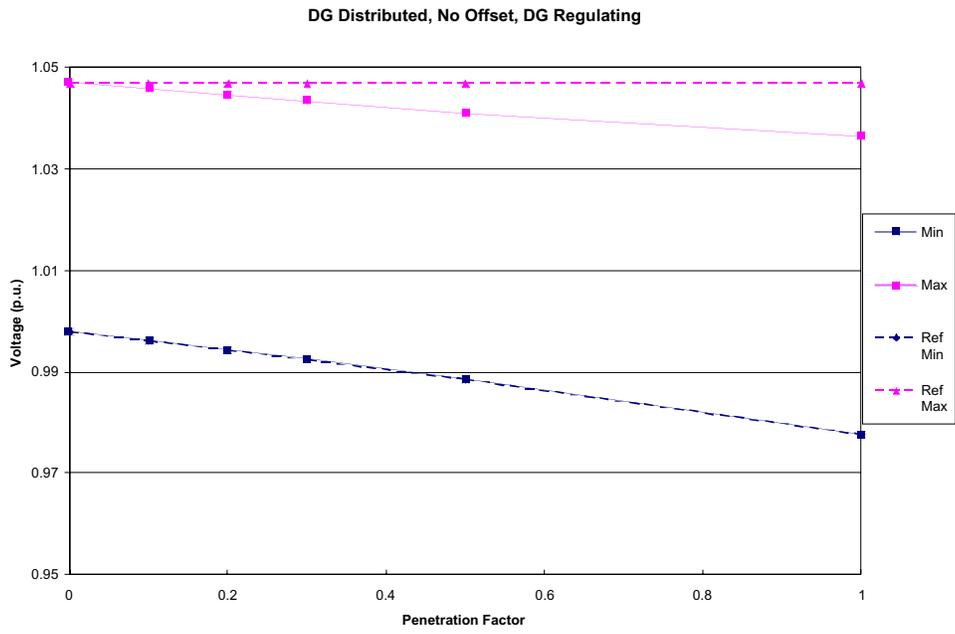
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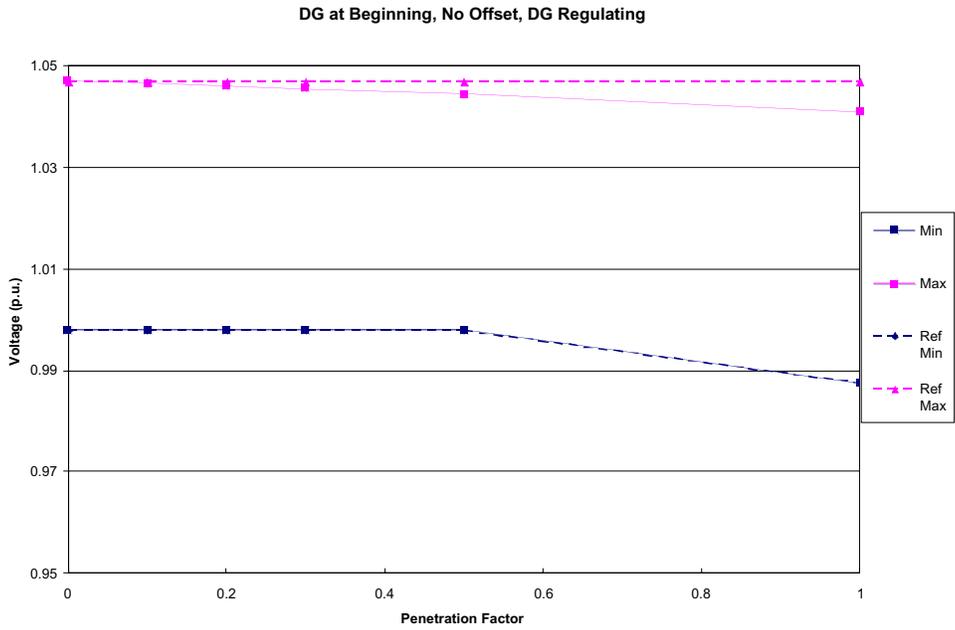
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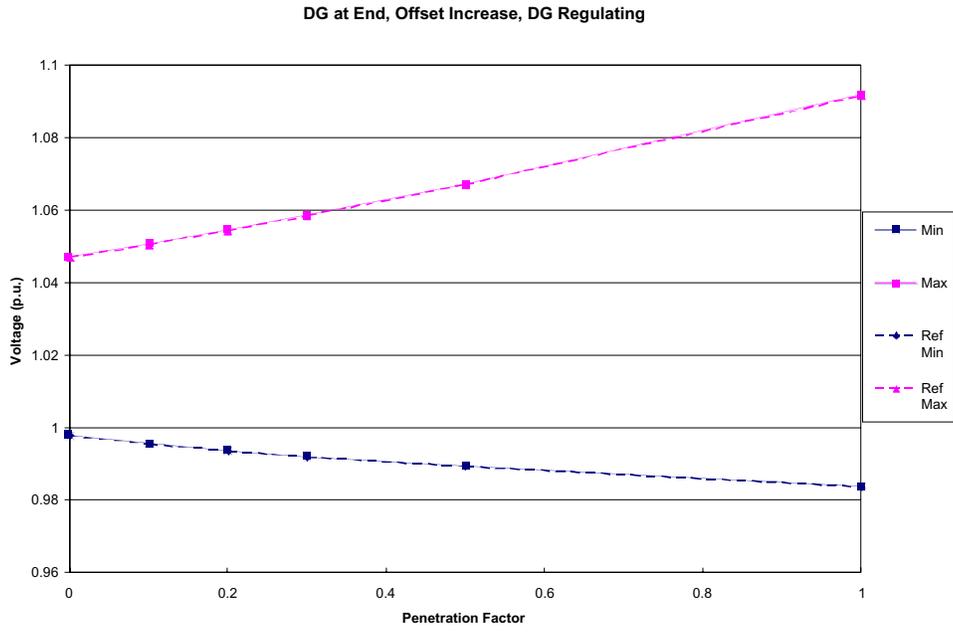
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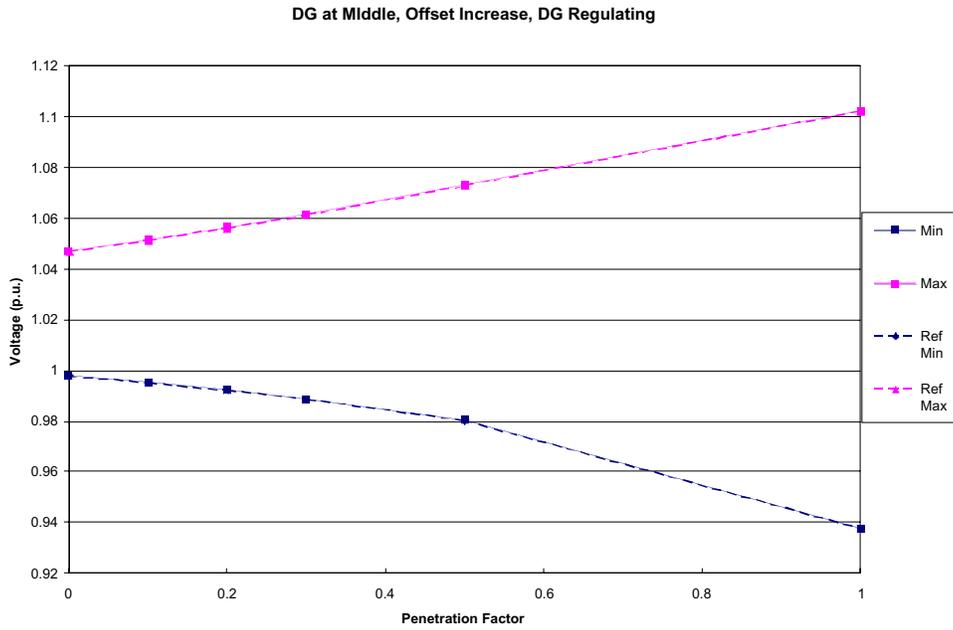
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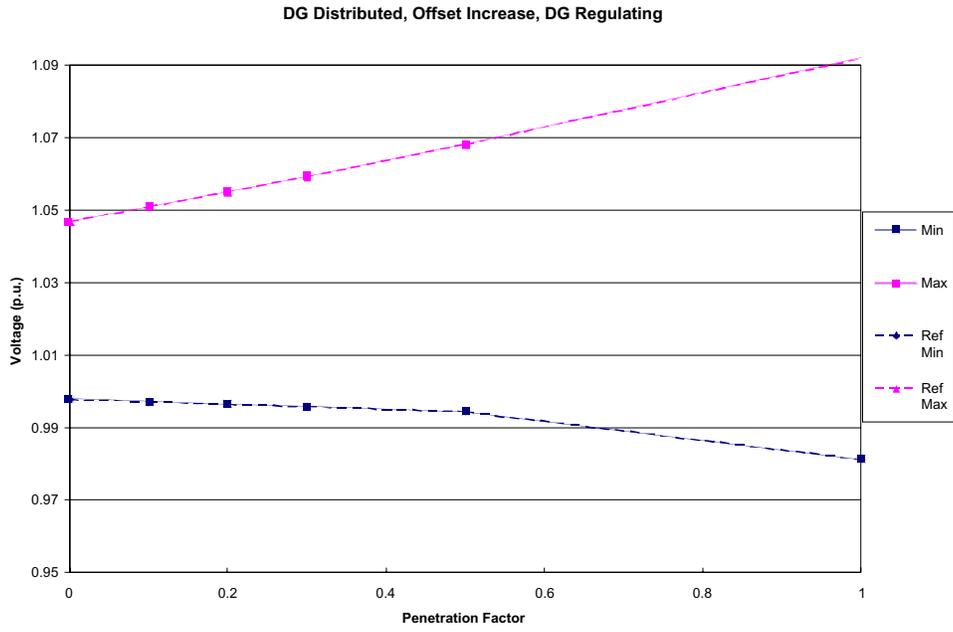
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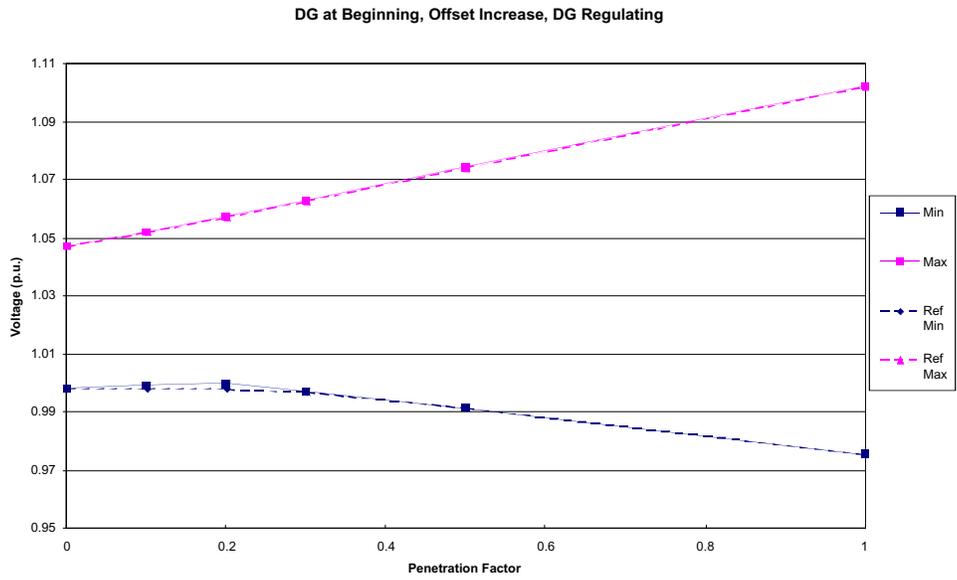
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### 3.1.2.2.3

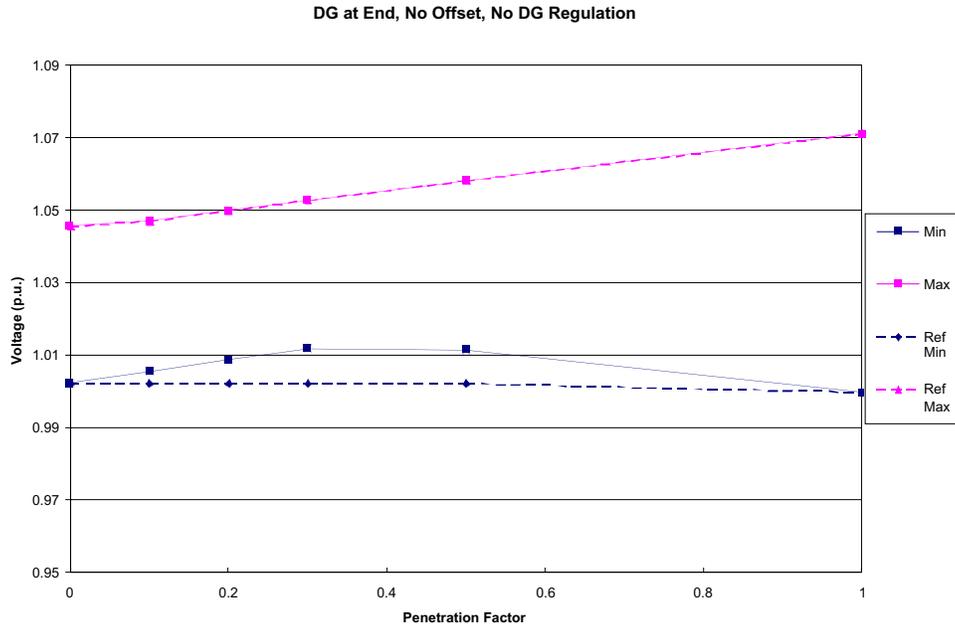


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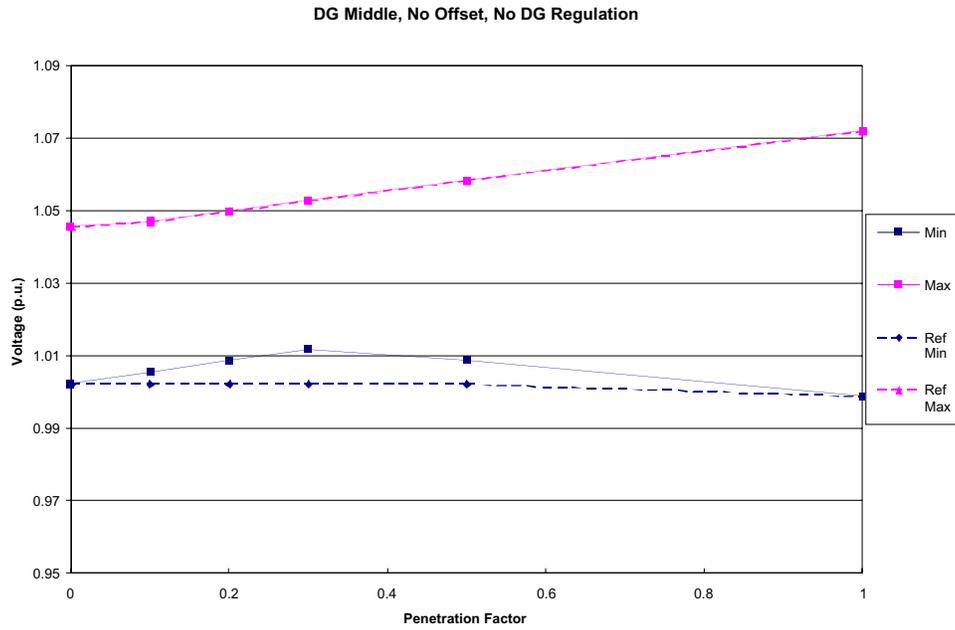


## BASE DESIGN 3.2

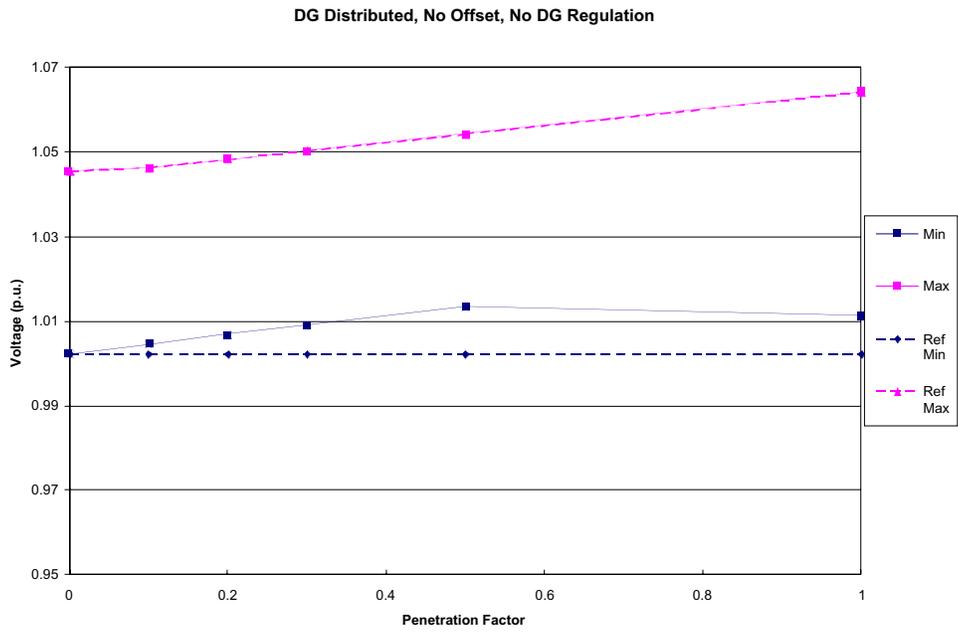
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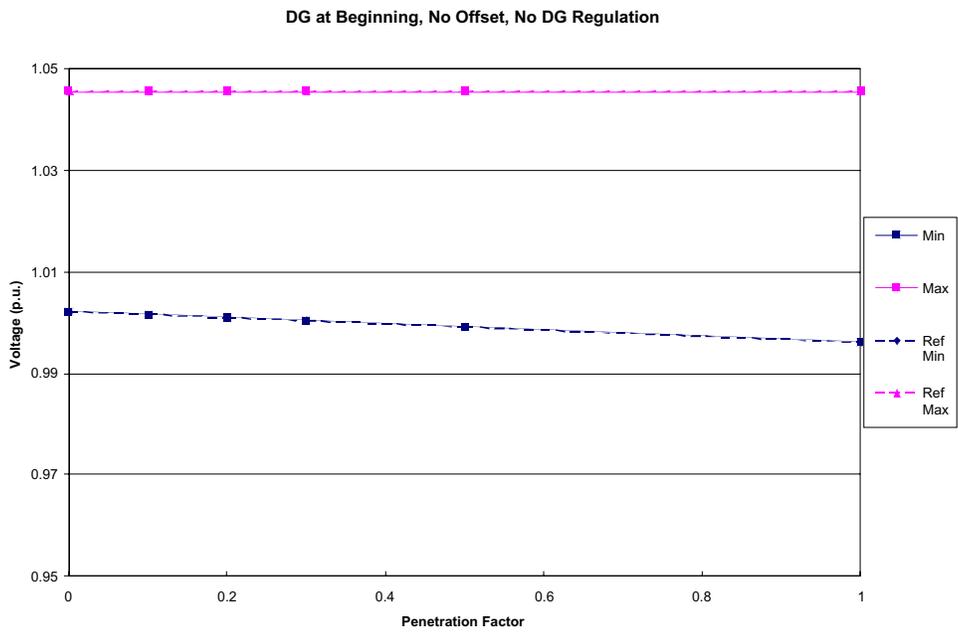
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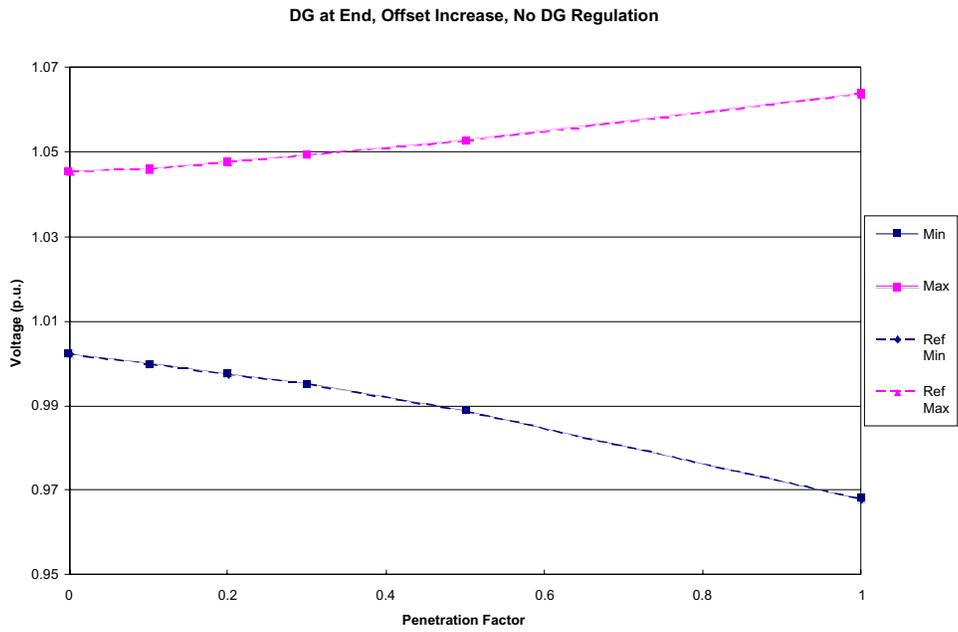
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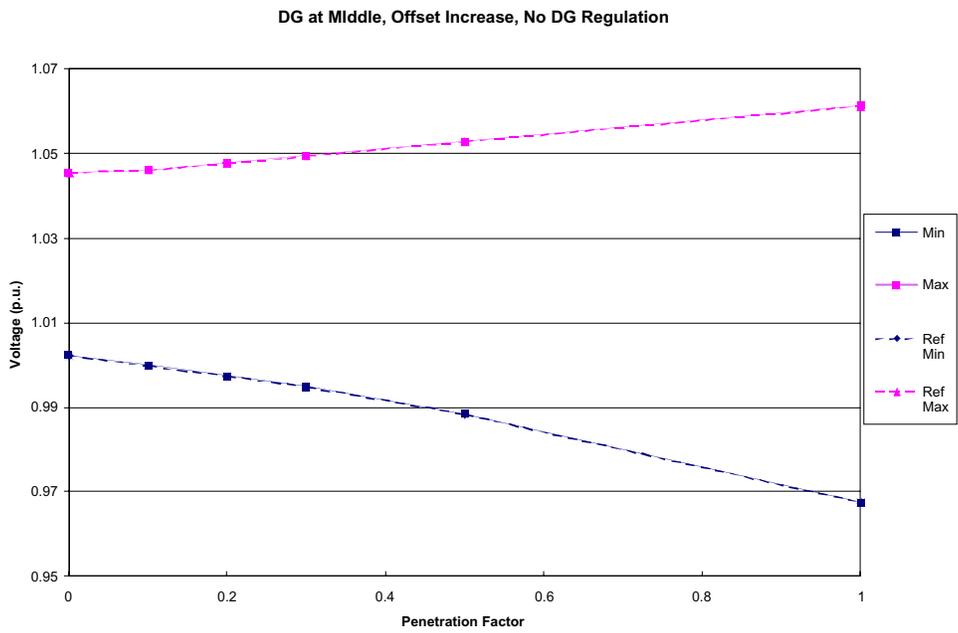
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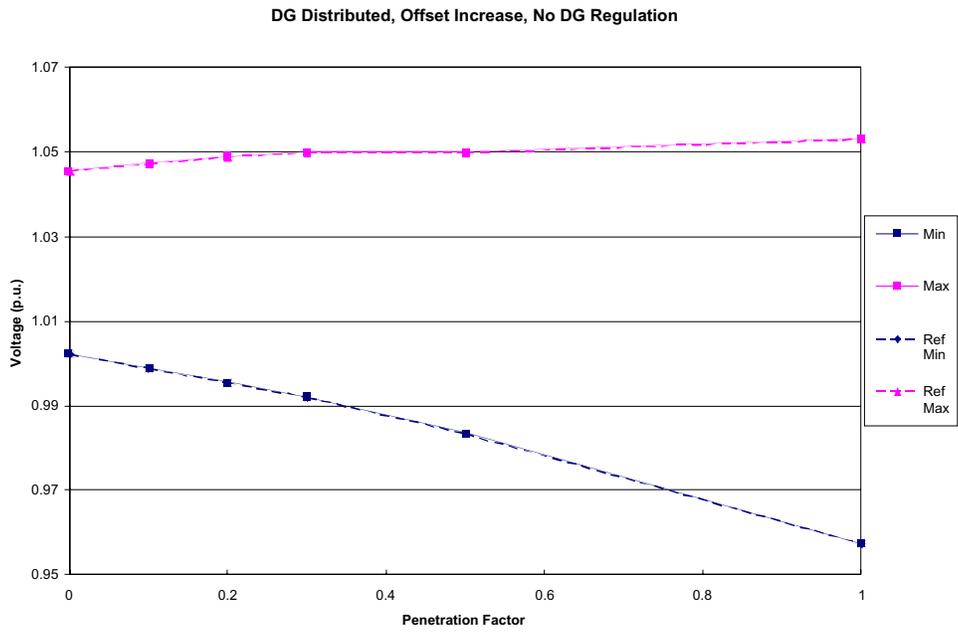
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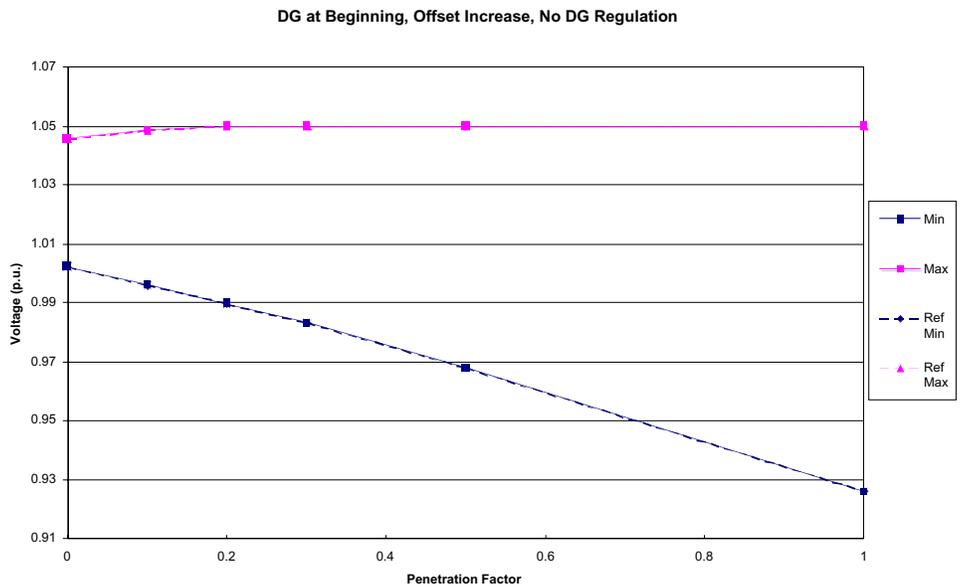
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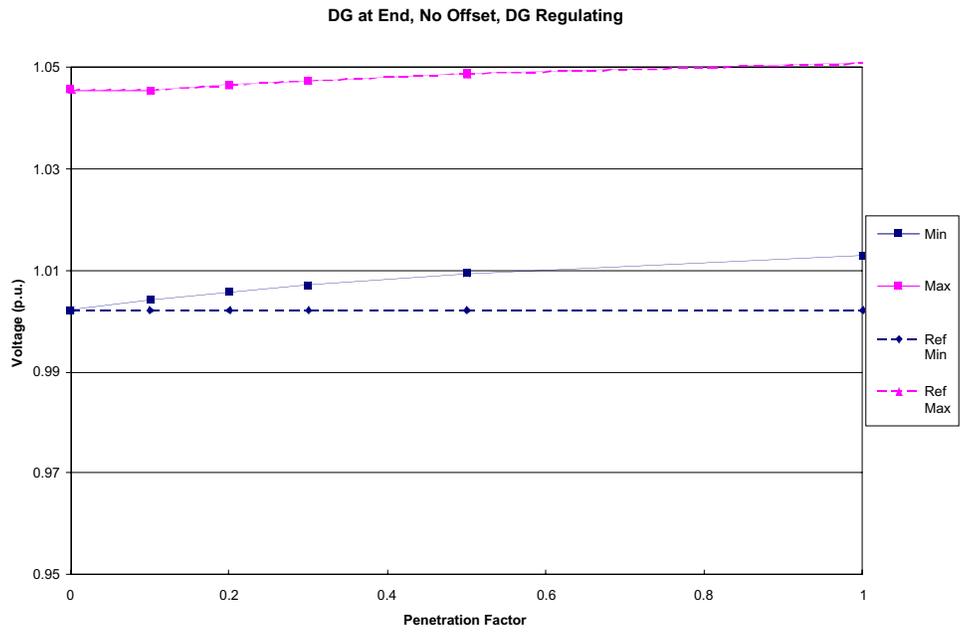
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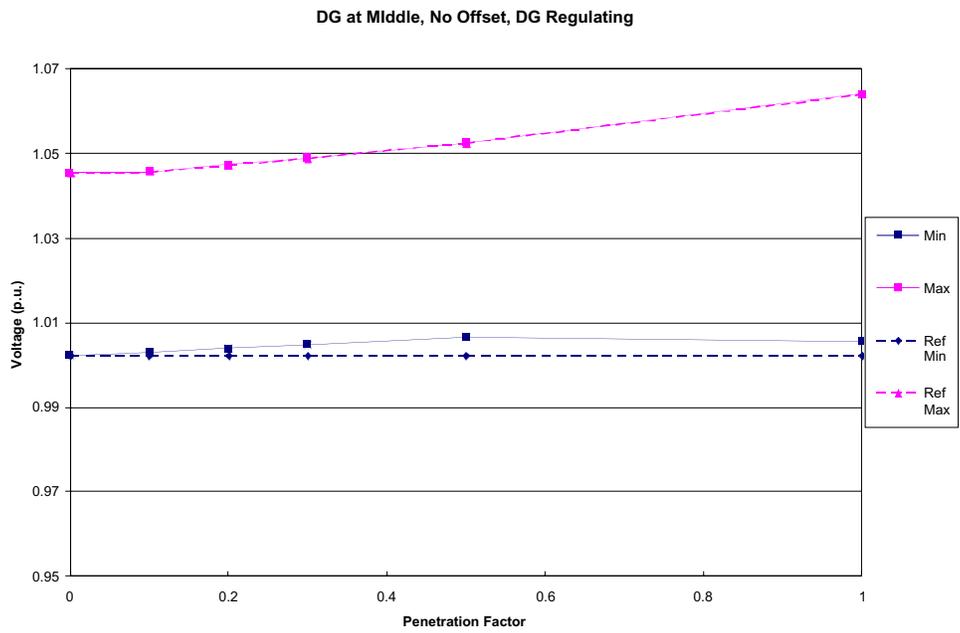
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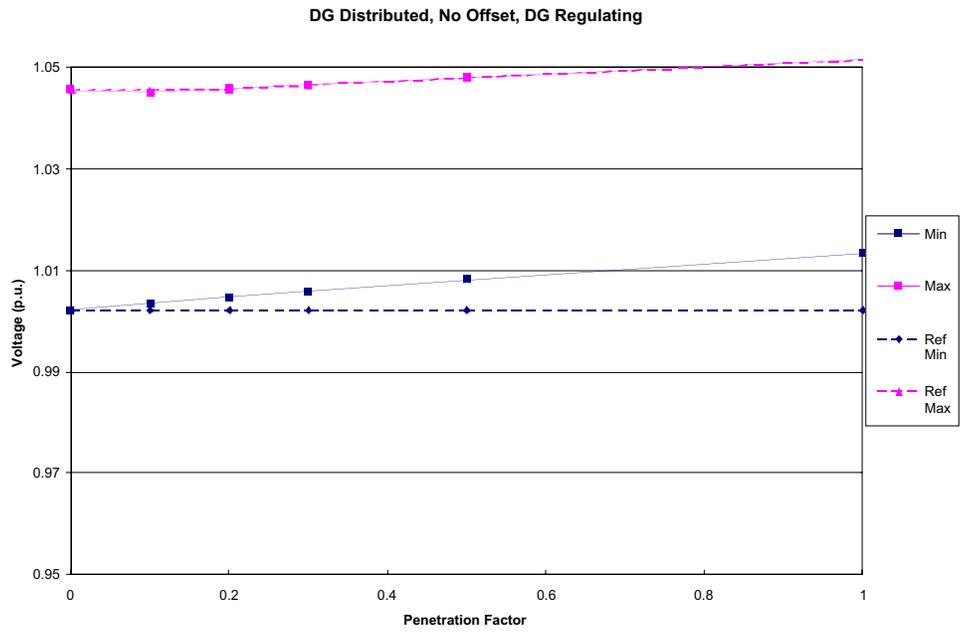
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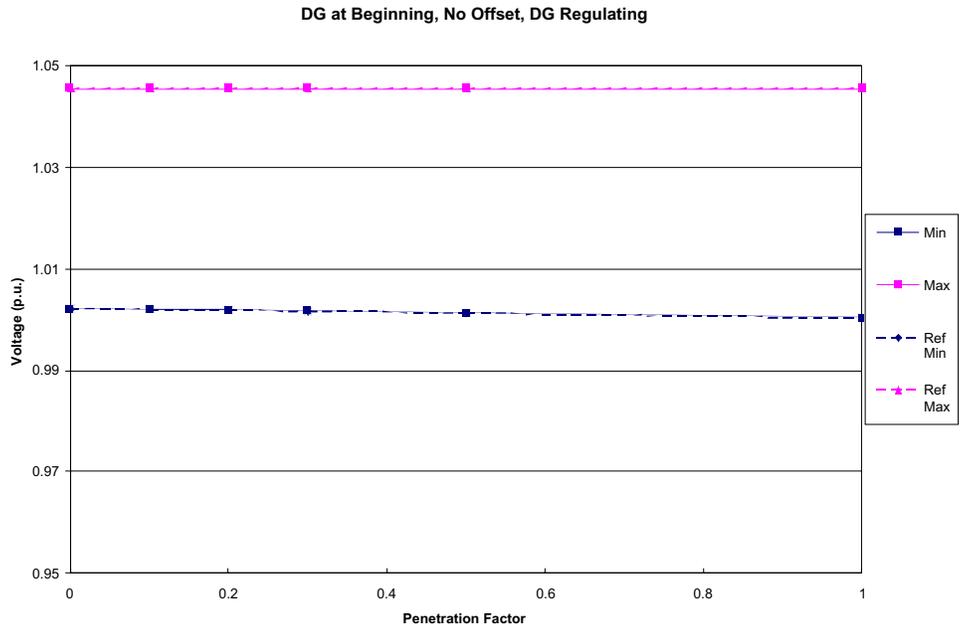
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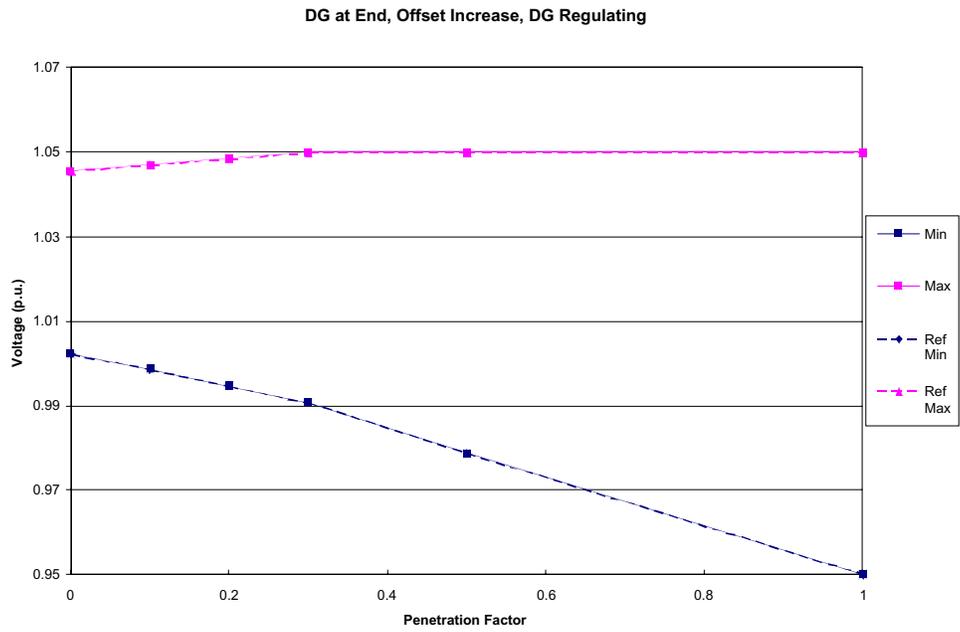
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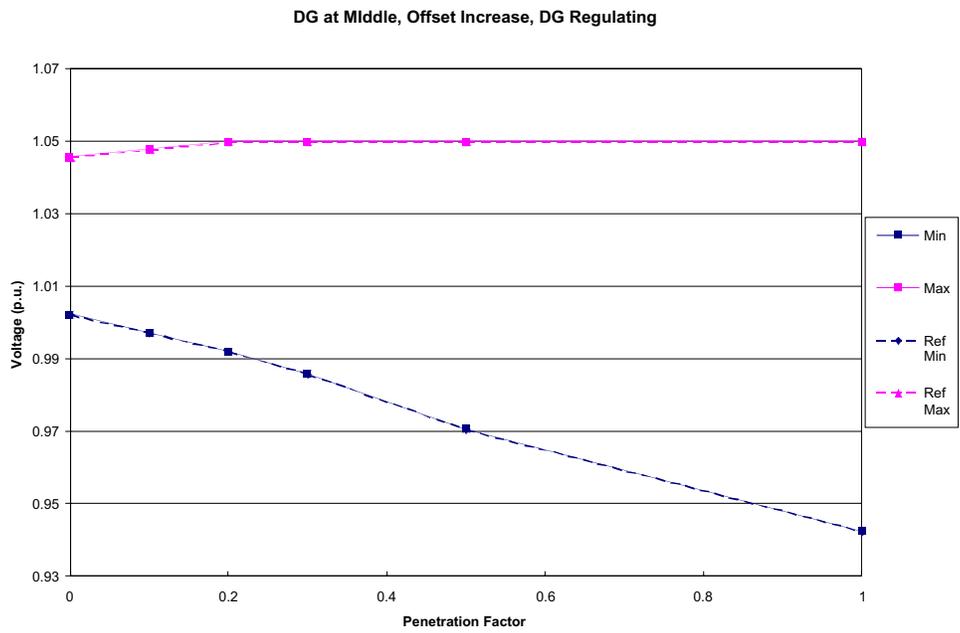
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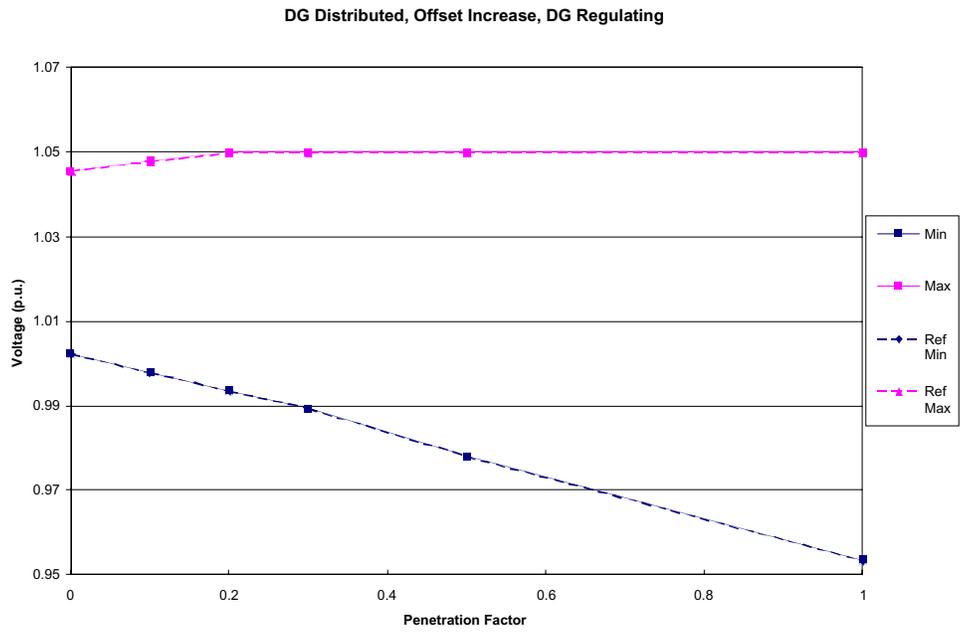
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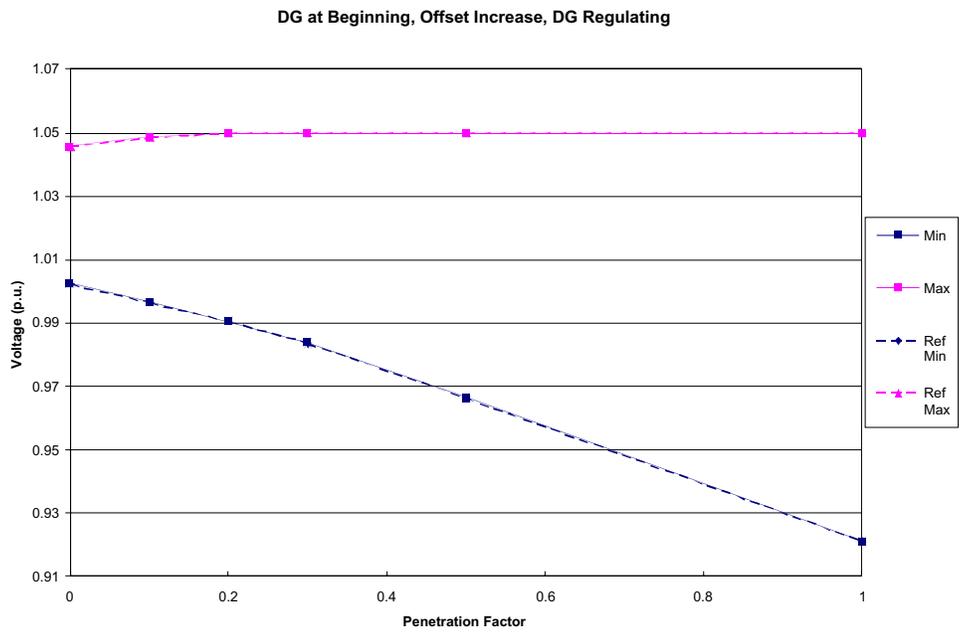
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### 3.2.2.2.3

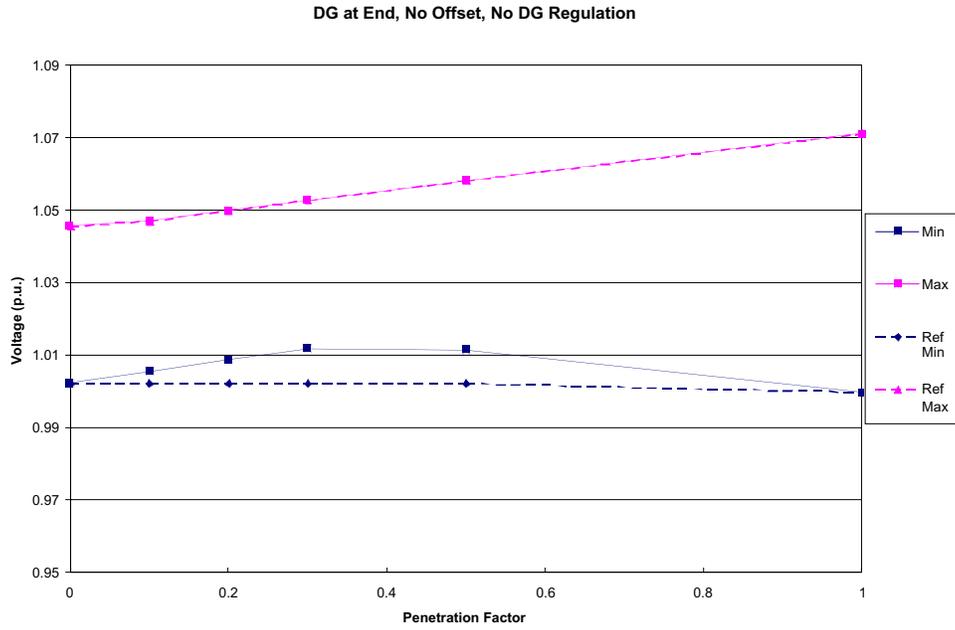


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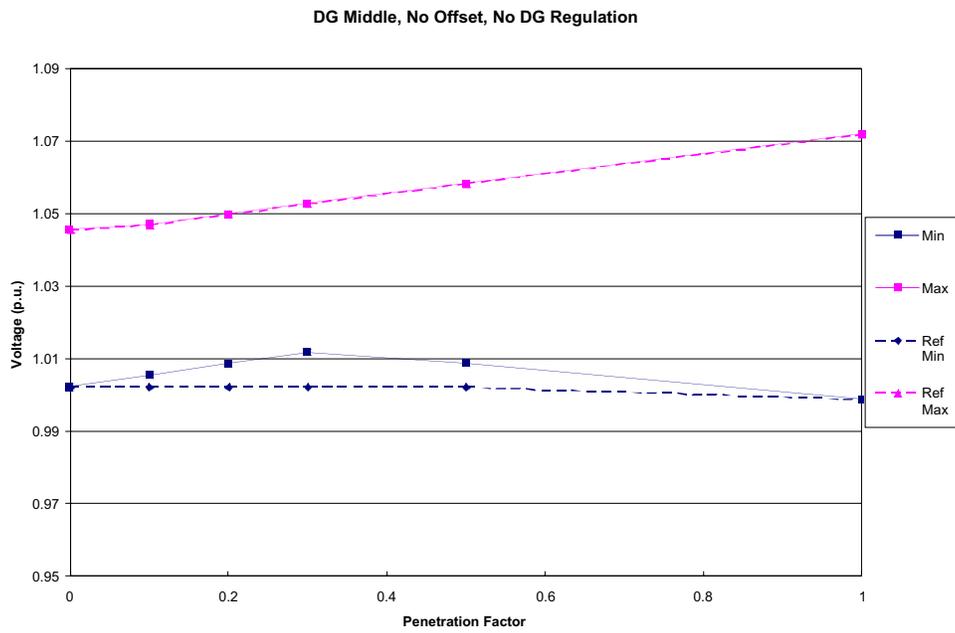


## BASE DESIGN 3.3

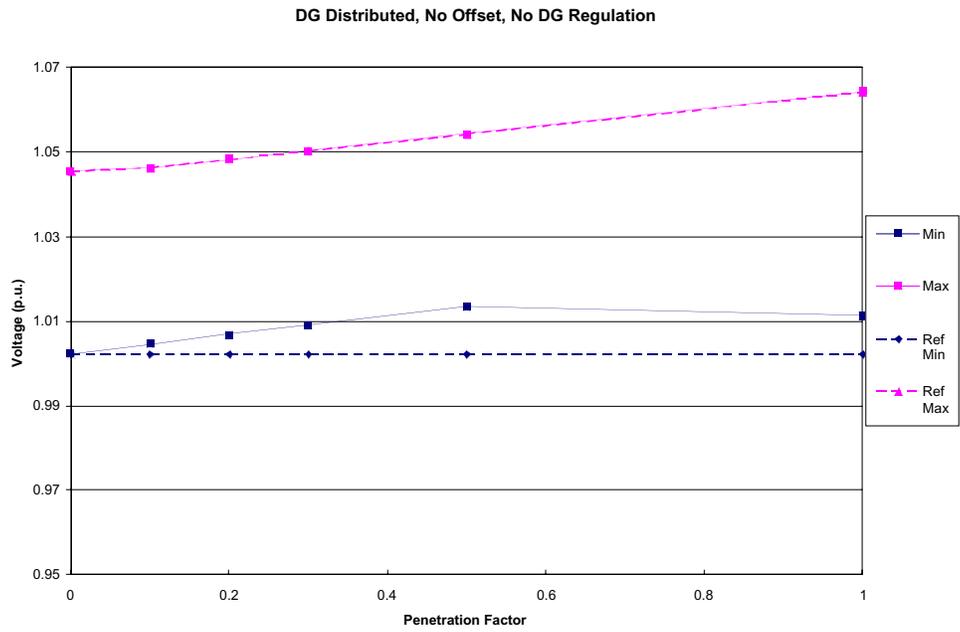
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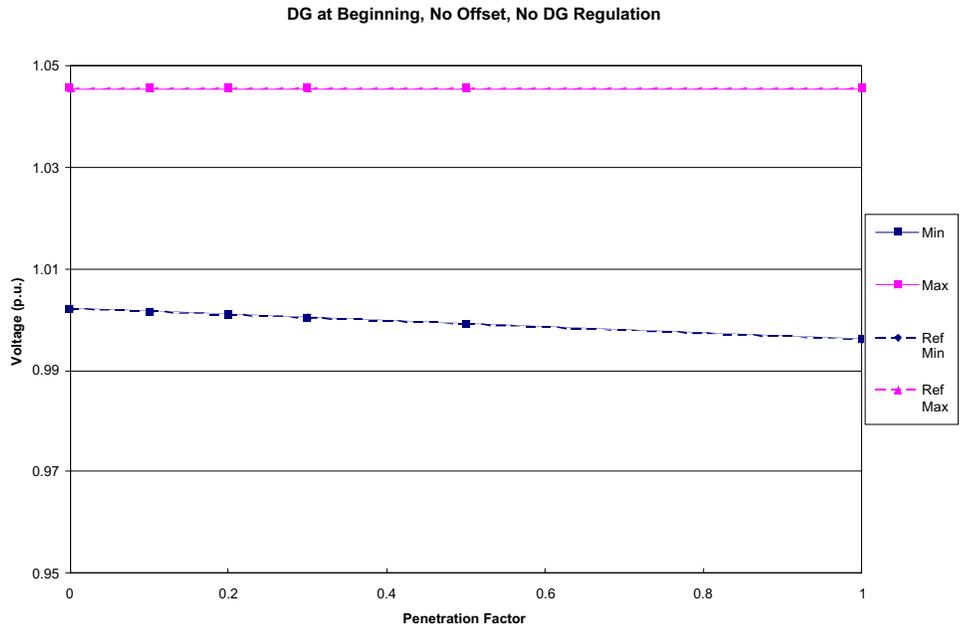
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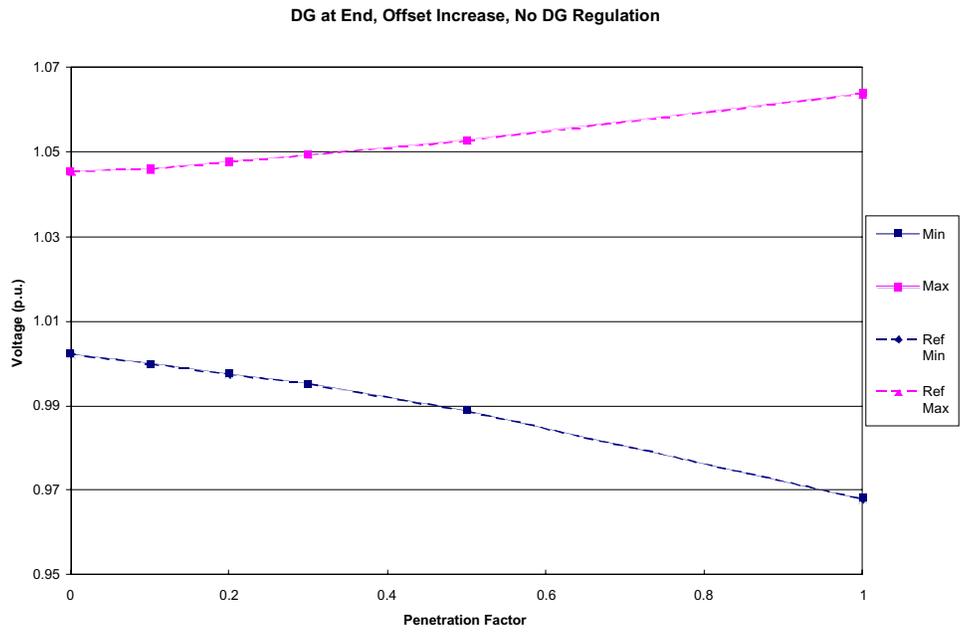
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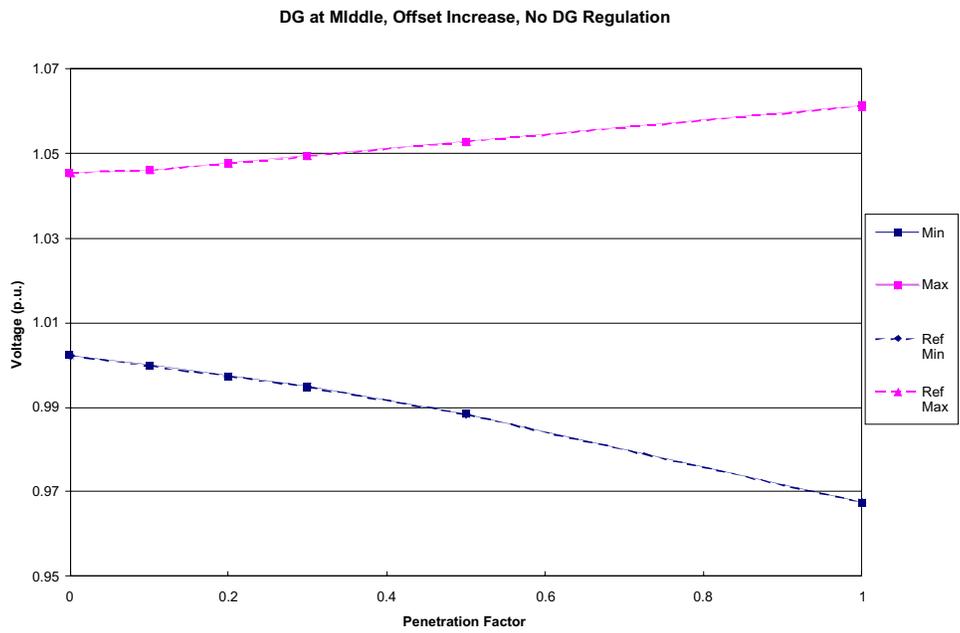
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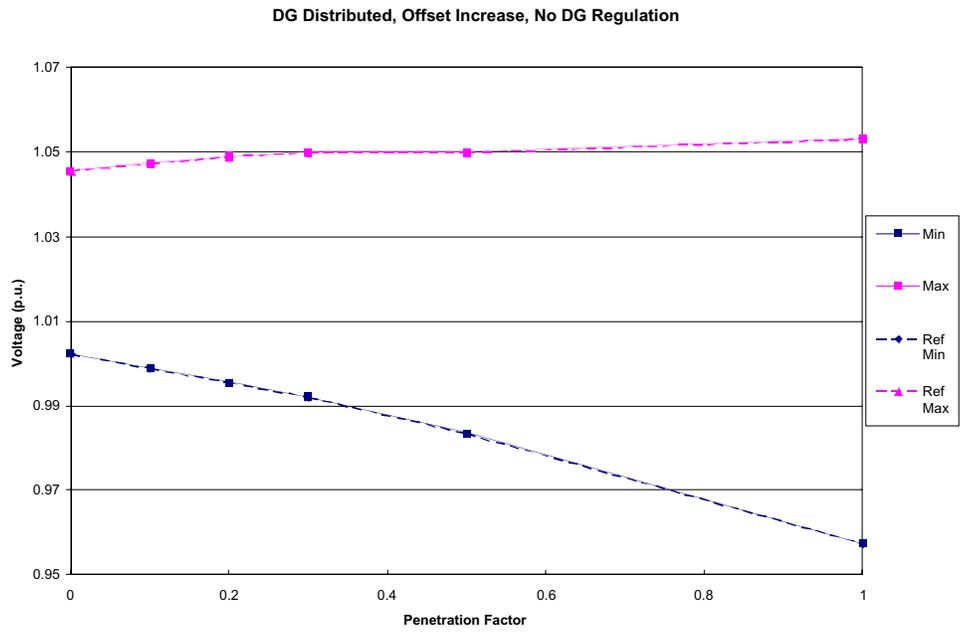
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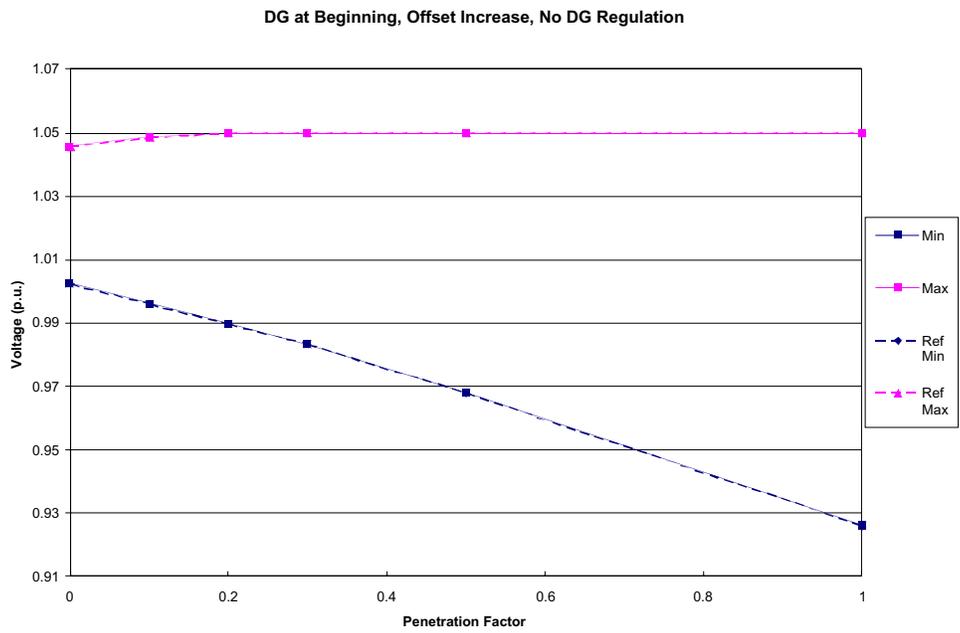
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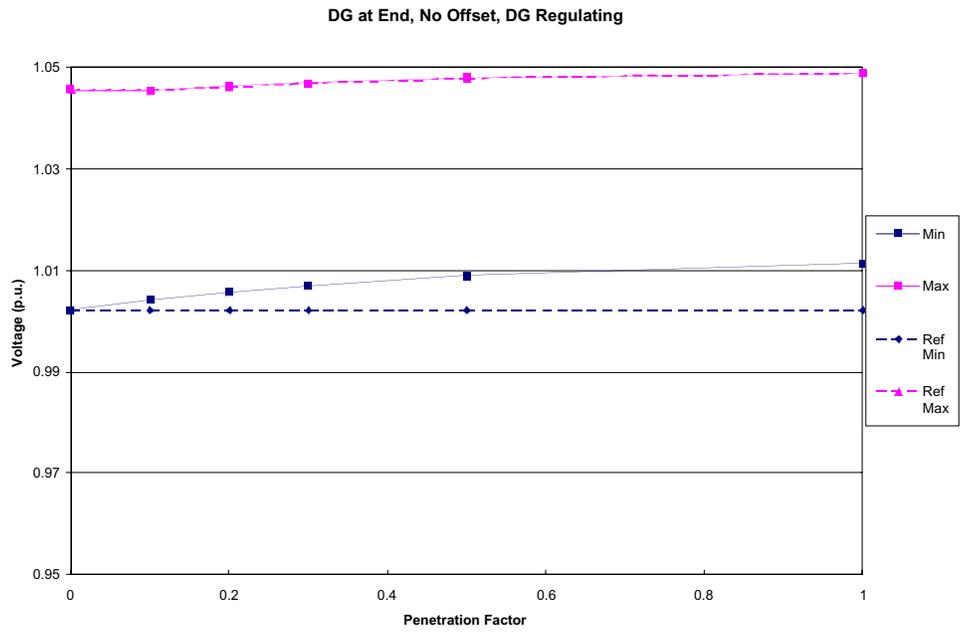
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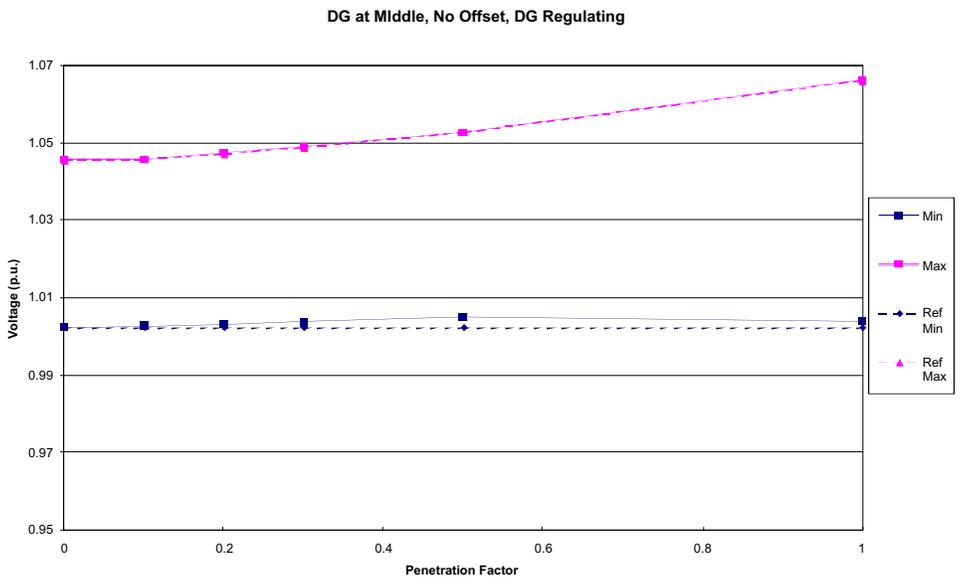
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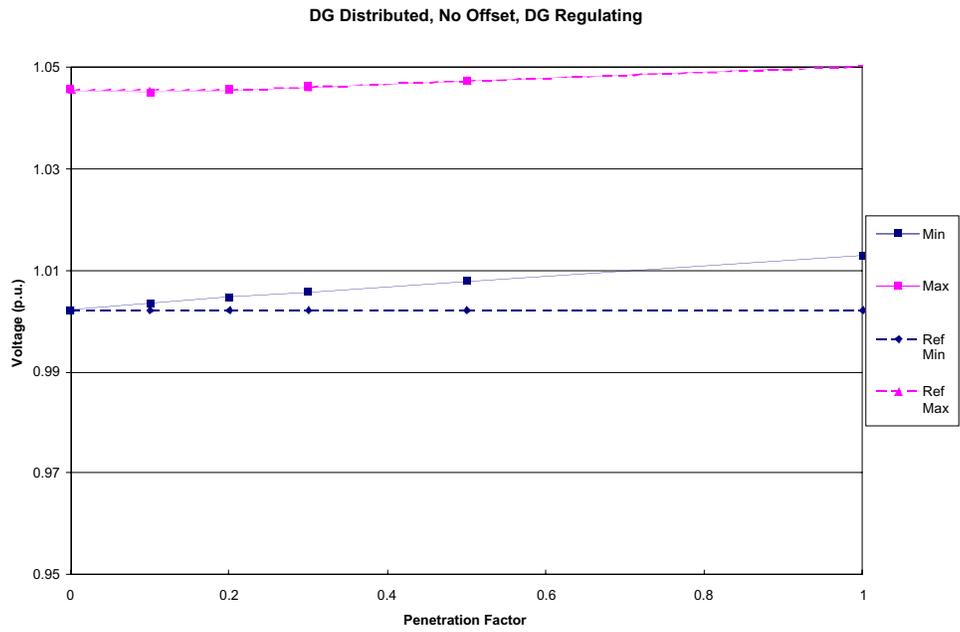
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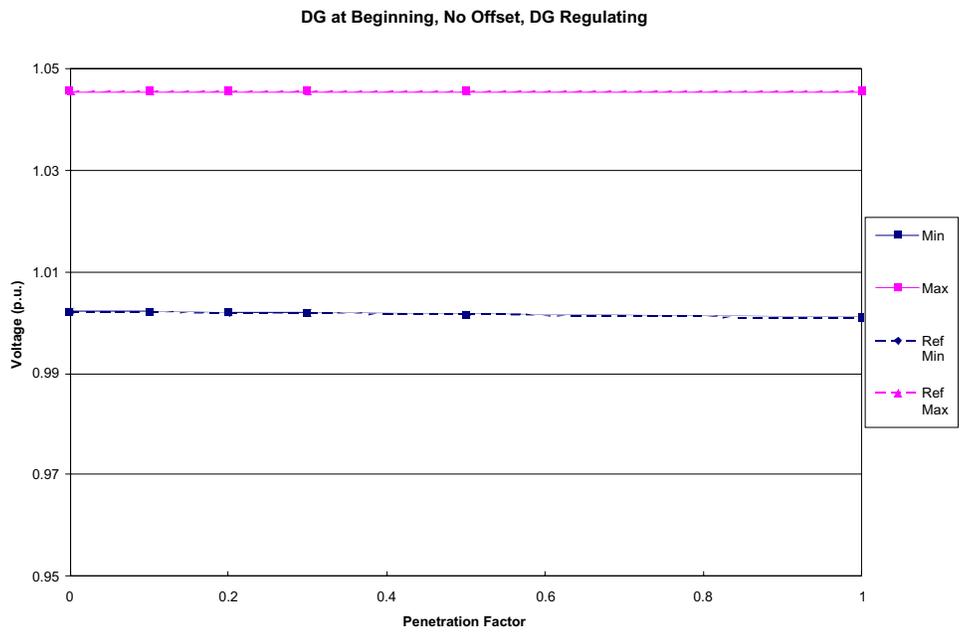
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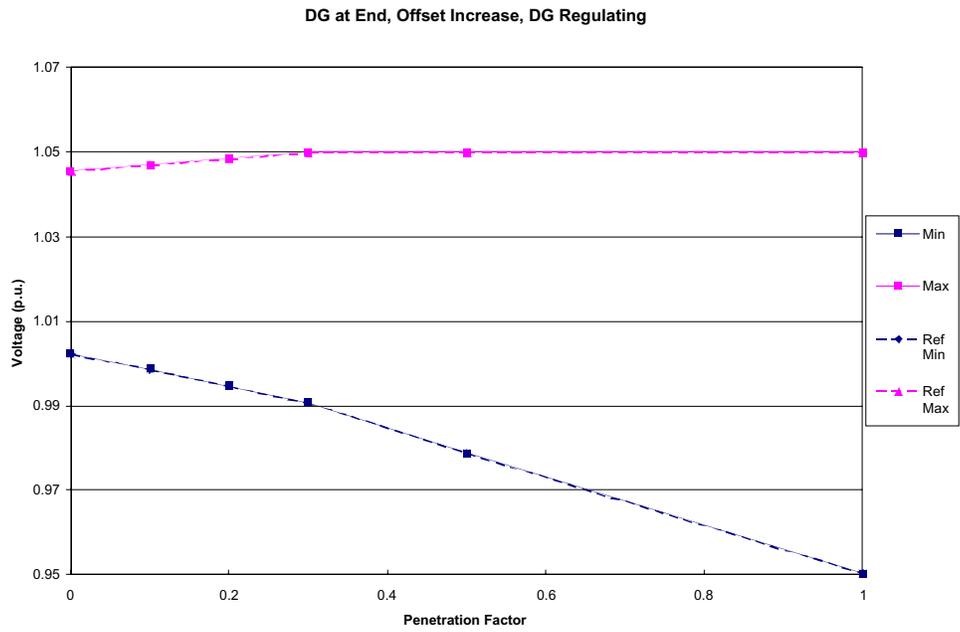
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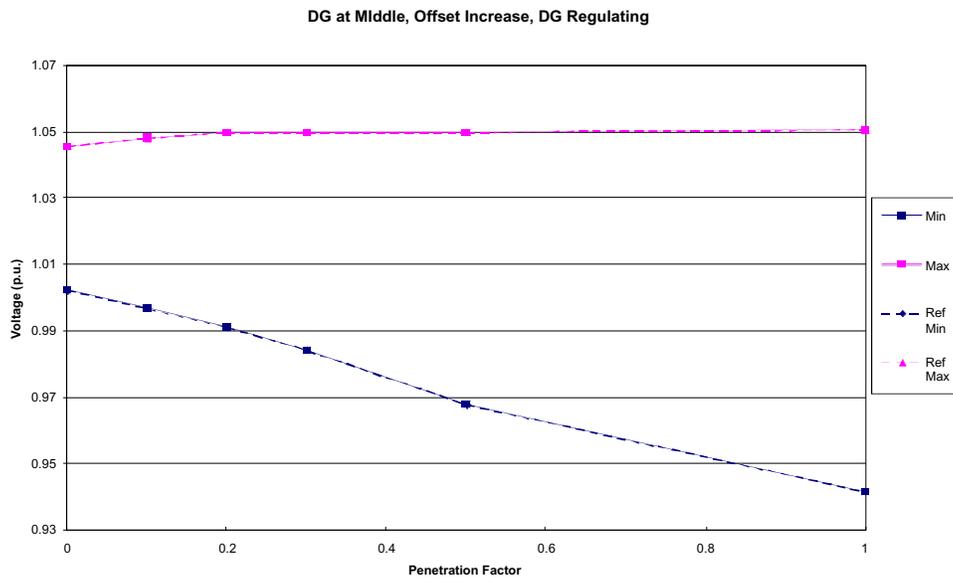
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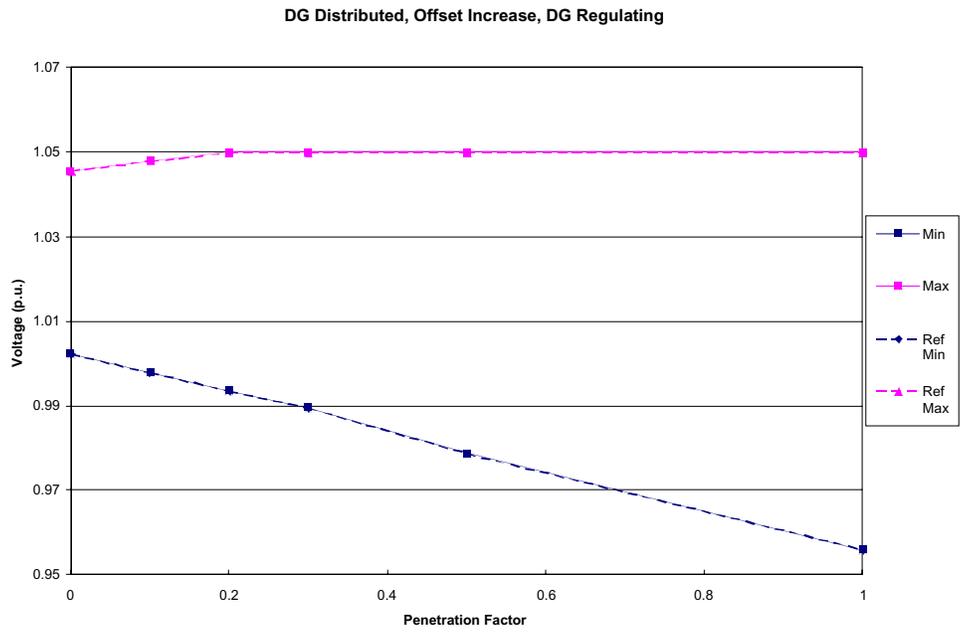
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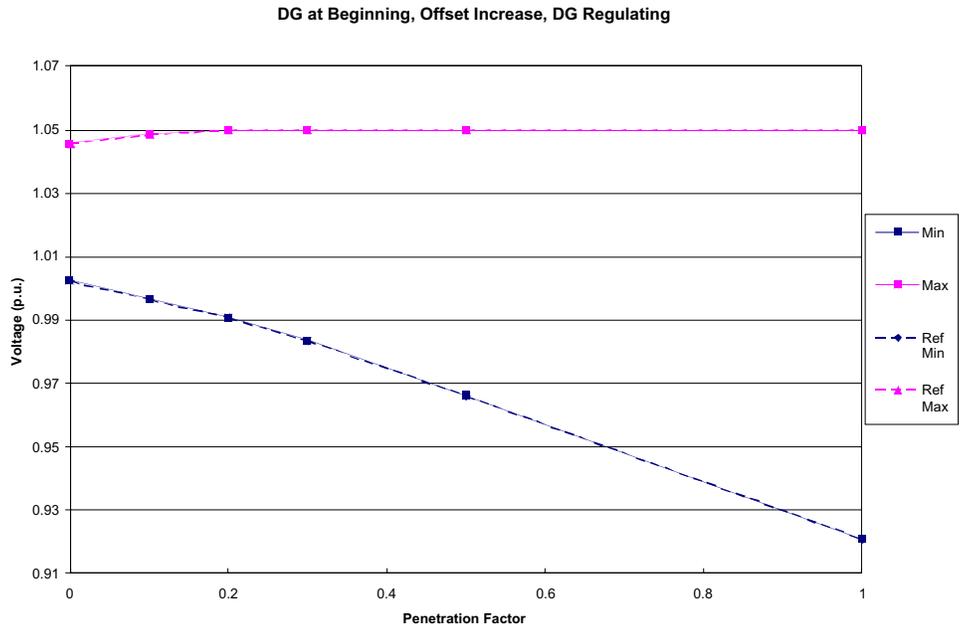
### 3.3.2.2.2



### 3.3.2.2.3



### 3.3.2.2.4



# Appendix B.

## Narrative Discussion of Generic Feeder Voltage Regulation Cases

### CASE 1.1

#### Description of the Feeder

**Feeder Length:** 4 miles

**LTC: Tap setting** = 1.05, Resistive LDC = 0.0, Reactive LDC = 0.0

**SVR:** None

**Capacitor Banks:** None

**Regulation Reference Point (when regulation is enabled):** DG voltage (secondary)

#### Scenario 1- Feeder load independent of DG penetration

(This scenario labeled No offset on the plots.)

For this scenario, the voltage regulation problems occur for the light load situation. An overvoltage problem occurs when the DG is lumped at the end (starting at a penetration factor of 20%) and the middle (30%) of the feeder. When the DG is lumped at the beginning and distributed throughout the feeder, no problem exists. When the DG is permitted to regulate its local voltage, the over voltage problem is eliminated for both DG at the end and middle.

There are no voltage regulations problems caused by DG penetration for the heavy load condition.

#### Scenario 2 — Peak feeder load increased by an amount equivalent to DG capacity ( Offset increase )

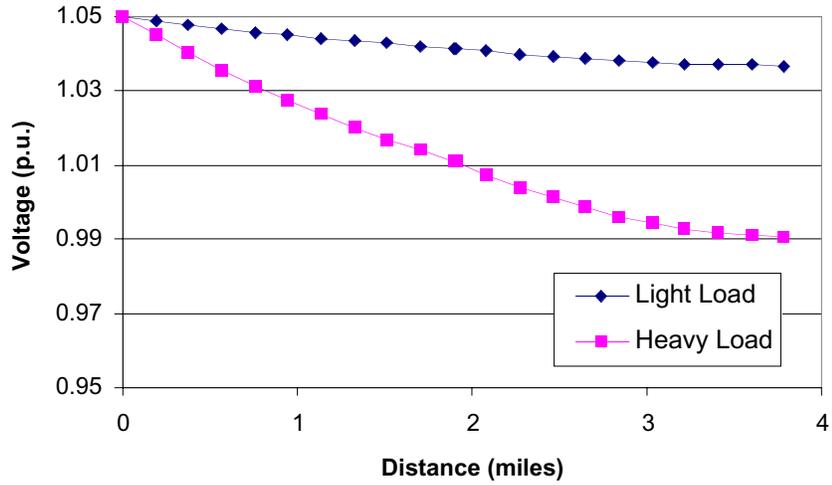
(This scenario labeled Offset increase on the plots.)

For the light load condition, there is only a minor overvoltage problem when the DG is lumped at the end of the feeder, but this problem occurs only for a very large penetration factor (100%). Therefore, it is not a major concern. Also, when voltage regulation is applied to the DG, this overvoltage is eliminated.

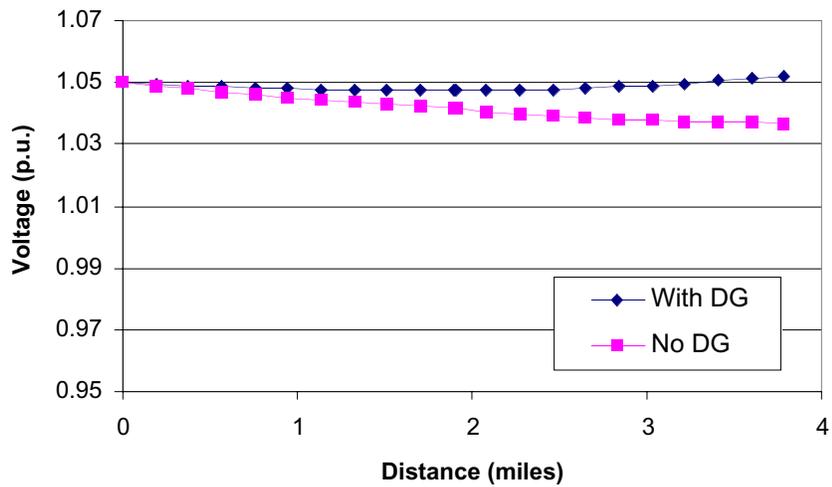
For the case of heavy load situation, a huge under-voltage occurs; particularly when the DG is lumped at the beginning (threshold at 20% penetration factor), but is least severe when the DG is lumped at the end (threshold between 50% and 100% penetration). This can be explained because the additional incremental load forces the system to supply the additional reactive power, increasing the voltage drop across the feeder. When the DG is situated at the beginning of the feeder, the power contribution from the DG and the grid add together to create a large voltage drop. Providing voltage regulation capability to the DG, within the typical DG reactive capacity constraints, does not mitigate this problem.

# CASE 1.1

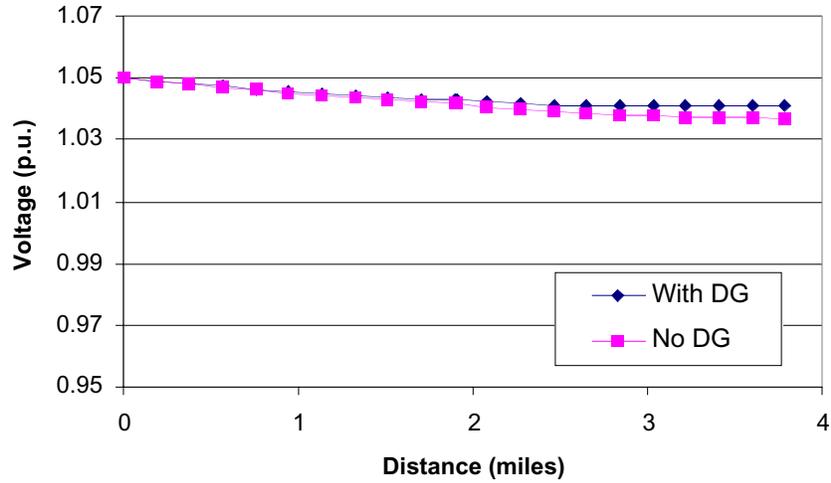
## Base Case (No DG)



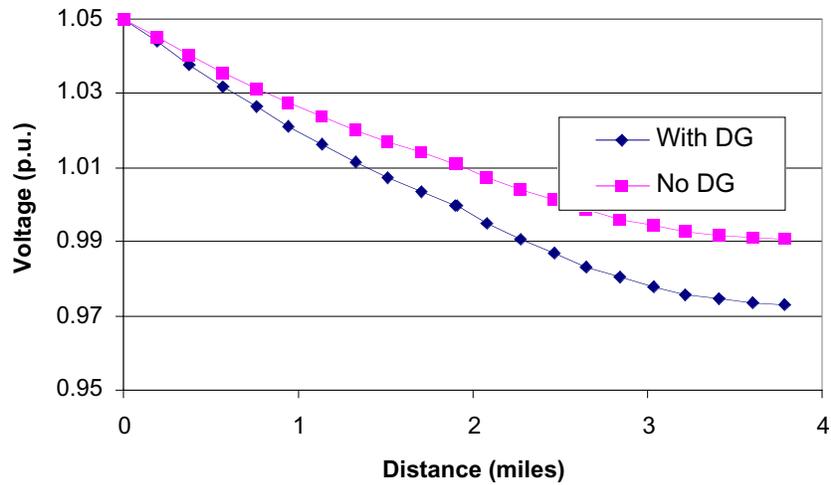
## Light Load, No offset, DG at the End, (30% Penetration)



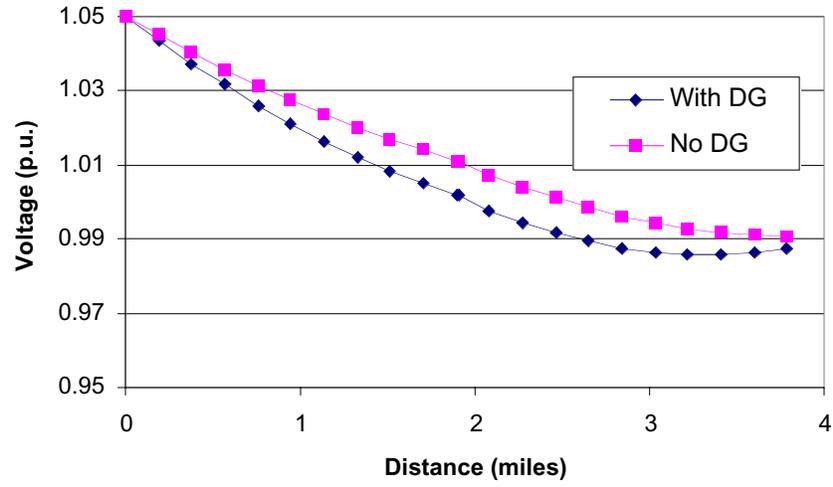
Light Load, No offset, Regulation, DG at the End, (30% Penetration)



Heavy Load, Offset increase, DG at the Beginning (30% Penetration)



Heavy Load, Offset increase, DG at the End, (50% Penetration)



## CASE 1.2

### Description of the Feeder

**Feeder Length:** 4 miles

**LTC: Tap setting** = 1.04, Resistive LDC = 0.3, Reactive LDC = 0.6, Max=1.05

**SVR:** None

**Capacitor Banks:** None

**Regulation Reference Point (when regulation is enabled):** DG voltage (secondary)

### Scenario 1- Feeder load independent of DG penetration

This scenario is similar to the situation in case 1.1 for light load, but the load drop compensation (LDC) in the LTC control helps improve the situation. With LDC, there is no overvoltage problem when the DG is lumped in the middle of the feeder. For the DG located at the end, the threshold of concern has been raised from 20% penetration in case 1.1 to between 30% and 50% penetration. The reason for this is that the DG is providing more power than the load demand for the light load case, and the substation source is absorbing power, the LTC load drop compensation works in a reversed way and reduces the voltage at the substation end. The decrease in substation voltage is sufficient to allow for the voltage rise along the feeder such that the voltage at the feeder end is in the acceptable range. Voltage regulation by the DG is effective in eliminating the overvoltage that do occur.

Like in case 1.1, there is no voltage regulation problem for the heavy load situation.

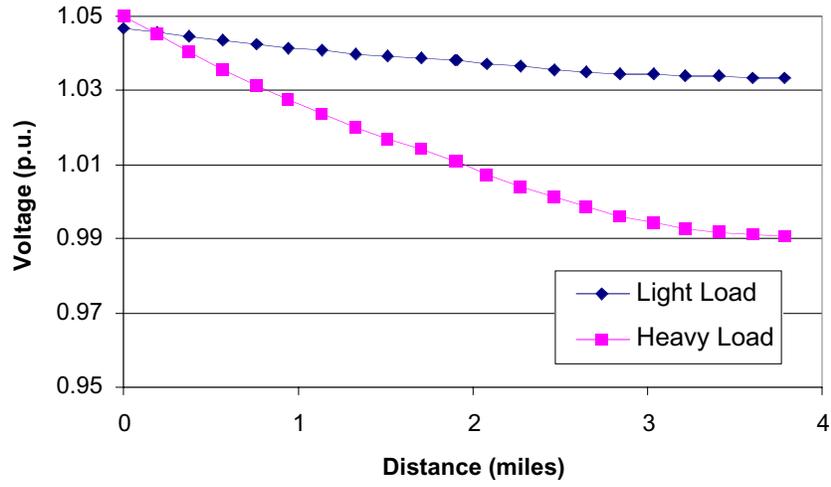
### Scenario 2 — Peak feeder load increased by an amount equivalent to DG capacity

The situation for the light load condition is very similar to case 1.1; overvoltage exists at the end of the feeder for very large (close to 100%) penetration. Also, when regulation by DG is applied, this small problem is eliminated.

For heavy load the situation does not change from case 1.1. Although load drop compensation was added, the LTC was locked to a maximum of 1.05 p.u. in order to not reach unacceptable overvoltage levels at loads close to the substation. Basically, the regulation by the LTC is the same as in case 1.1, and voltage regulation is not an adequate mitigant.

# CASE 1.2

## Base Case (No DG)



Light Load, No offset, Regulation, DG at the End (30% Penetration)

## CASE 1.3

### Description of the Feeder

**Feeder Length:** 4 miles

**LTC: Tap setting** = 1.05, Resistive LDC = 0.0, Reactive LDC = 0.0

**SVR:** None

**Capacitor Banks:** 4 banks located at 20%, 40%, 60% and 80% of the feeder length.

Each bank supplies  $\frac{1}{4}$  of the additional reactive power due to the incremental load, which depends on penetration factor and the power factor of the load. The compensation is fixed for each penetration level, and based on rated peak load. Thus, the compensation is present for the light load as well as heavy load situation, representing a compensation design using fixed capacitor banks.

**Regulation Reference Point (when regulation is enabled):** DG voltage (secondary)

### Scenario 1- Feeder load independent of DG penetration

In this case, capacitors were added only in proportion to the incremental load added with increased DG penetration. In this scenario, feeder loads are fixed. Thus, for this scenario, results are the same as in Case 1.1.

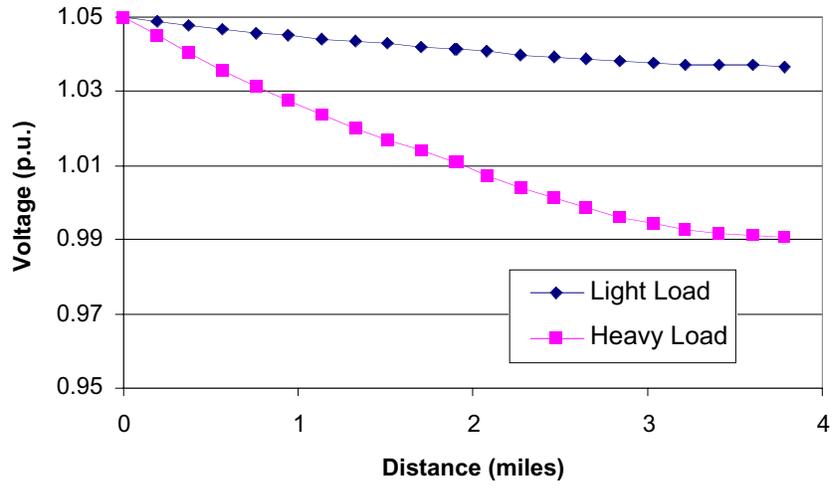
### Scenario 2 — Peak feeder load increased by an amount equivalent to DG capacity

For the light load case, the capacitor aggravate the overvoltage problem. Instead of only overvoltage problems being limited to the situation where the DG is located at the end of the feeder, overvoltages also occur when the DG is located in the middle of the feeder, or when the DG is uniformly distributed. However, when DG voltage regulation is enabled, this overvoltage problem is eliminated.

For the heavy load situation, providing incremental rective compensation helps, but this measure is not sufficient to avoid serious undervoltage problems.

# CASE 1.3

## Base Case (No DG)



## CASE 2.1

### Description of the Feeder

**Feeder Length:** 8 miles

**LTC: Tap setting** = 1.01, Resistive LDC = 0.75, Reactive LDC = 1.5

**SVR:** None

**Capacitor Banks:** 900 kVA banks located at 20%, 40%, 60% and 80% of the feeder length.

**Regulation Reference Point (when regulation is enabled):** DG voltage (secondary)

### Scenario 1- Feeder load independent of DG penetration

For light load, the load drop compensation reduces the voltage at the substation end. Because of the high LDC settings, undervoltage problems occur for all the tested DG locations, starting at a 50% DG penetration factor. Also, above a 50% penetration, there is an overvoltage problem when the DG is at the remote end of the feeder. Allowing regulation by the DG increases the threshold of voltage regulation problems to between 50% and 100% penetration for all DG locations other than DG at the beginning of the feeder. With the DG at the beginning, the undervoltage problem becomes more severe when DG voltage regulation is included.

When the feeder is heavily loaded, the load drop compensation is effective in minimizing undervoltage problems. Undervoltage occurs only when the DG is at the beginning with very large penetration factors. Voltage regulation by the DG solves this problem.

### Scenario 2 — Peak feeder load increased by an amount equivalent to DG capacity

For the light load situation, there are no voltage regulation problems.

The incremental load results in severe voltage regulation problems when the system is heavily loaded. First, due to the load drop compensation on the LTC, there are overvoltage problems for any penetration factor greater than zero, and for all DG locations. Additionally, this excessive boost at the LTC is still not enough to compensate for the voltage drop across the feeder. This results in undervoltage problems, particularly when the DG is located at the beginning. Only when the DG is at the end is this undervoltage problem not present. Regulation by the DG is not effective in mitigating these problems.

## CASE 2.2

### Description of the Feeder

**Feeder Length:** 4 miles

**LTC: Tap setting** = 1.02, Resistive LDC = 0.6, Reactive LDC = 1.1 Max=1.05

**SVR:** None

**Capacitor Banks:** 1200 kVA banks located at 20%, 40%, 60% and 80% of the feeder length.

**Regulation Reference Point (when regulation is enabled):** DG voltage (secondary)

### Scenario 1- Feeder load independent of DG penetration

Light load: By reducing the load drop compensation and increasing the capacitive compensation, the undervoltage problem of case 2.1 at the substation is almost eliminated (little under-voltage at 100% penetration for all locations). However, there now exists an even larger overvoltage at the remote end of the feeder with lower penetration thresholds (end: 20%, middle: 30-50%, distributed: 30-50%). Applying DG voltage regulation eliminates the overvoltage problem.

Heavy Load: Similar to case 2.1.

### Scenario 2 — Peak feeder load increased by an amount equivalent to DG capacity

Light Load: Large overvoltages appear at 20% penetration when the DG is located at the end. DG regulation eliminates this problem.

Heavy Load: By setting a maximum to the LTC voltage, the overvoltage problem of Case 2.1 is eliminated. However, this increases the undervoltage problem that occurs at every location of the DG (50% penetration for DG at the feeder end, 20% middle, 20% distributed, 10% beginning). When the DG is located at the beginning, the undervoltage is very severe. At the remote end of the feeder, the voltage drops as low as 0.87 p.u. Voltage regulation does not eliminate the problem.

## CASE 3.1

### Description of the Feeder

**Feeder Length:** 8 miles

**LTC: Tap setting** = 1.02, Resistive LDC = 0.5, Reactive LDC = 1

**SVR: Tap setting** = 1.01, Resistive LDC = 1.0, Reactive LDC = 2.0

**Capacitor Banks:** 900 kVA banks located at 20%, 40%, 60% and 80% of the feeder length.

**Regulation Reference Point (when regulation is enabled):** DG voltage (secondary)

### Scenario 1- Feeder load independent of DG penetration

For the light load situation, there is no overvoltage problem due to the corrective action of the load drop compensation. Instead, undervoltages occur at the feeder location immediately after the SVR when the DG is located at the middle and at the end for large penetration factors (threshold of concern is 50% penetration). This can be attributed to the excessive load drop compensation of the SVR and to the direction of the real power at that location. When the DG is located at the end and the middle (both locations are after the SVR) the flow of real power is high in the direction of the substation, so the real component of the drop compensation at the SVR reduces the voltage significantly. Additionally, there is also flow of reactive power (supplied by the cap banks) in that direction at the SVR location, which makes the reactive component of the drop compensation to further reduce the voltage at that point. When the DG is distributed, or at the beginning, there is no undervoltage since the real flow is now reversed. Regulation by the DG does not eliminate the problem. For the DG located at the middle of the feeder, regulation of the DG secondary voltage toward a 1.0 p.u. setpoint aggravates the problem.

For the heavy load situation, there is no voltage regulation issue.

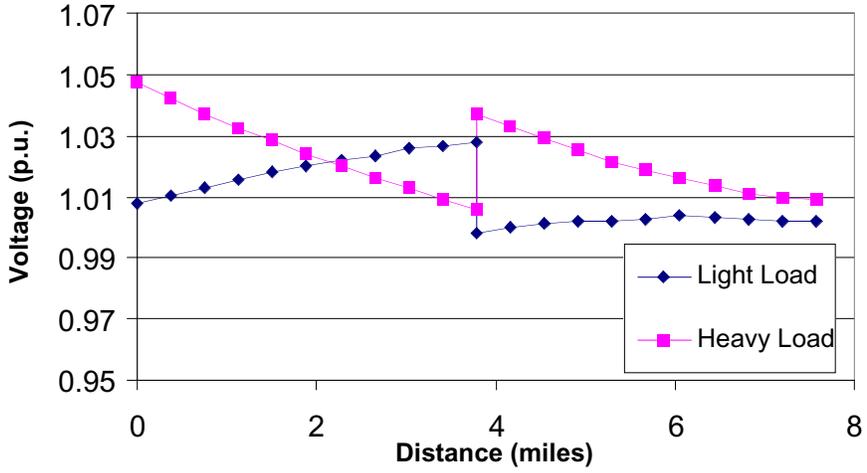
### Scenario 2 — Peak feeder load increased by an amount equivalent to DG capacity

For the light load situation, there is also an undervoltage problem when DG is at middle or at the end, but the undervoltage problem is less severe than in Scenario 1 for this case (threshold penetration is almost 100%). DG regulation eliminates the undervoltage when the DG is at the end, but makes the situation worse when DG is at the middle.

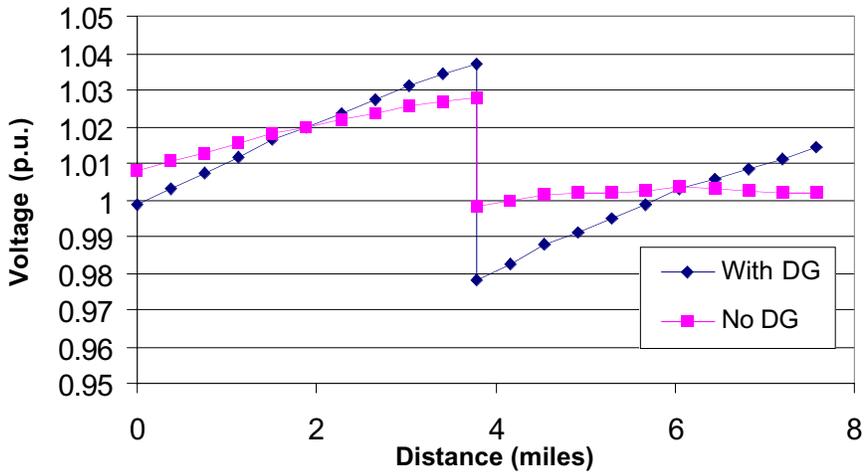
For the heavy load situation, there is an overvoltage problem for any DG location and for any significant penetration factor. This occurs due to an excessive boost at the substation end by the LTC load drop compensation, and the fact that the LTC was limited to a maximum value in this case. Implementing DG voltage regulation aggravates this overvoltage problem.

### CASE 3.1

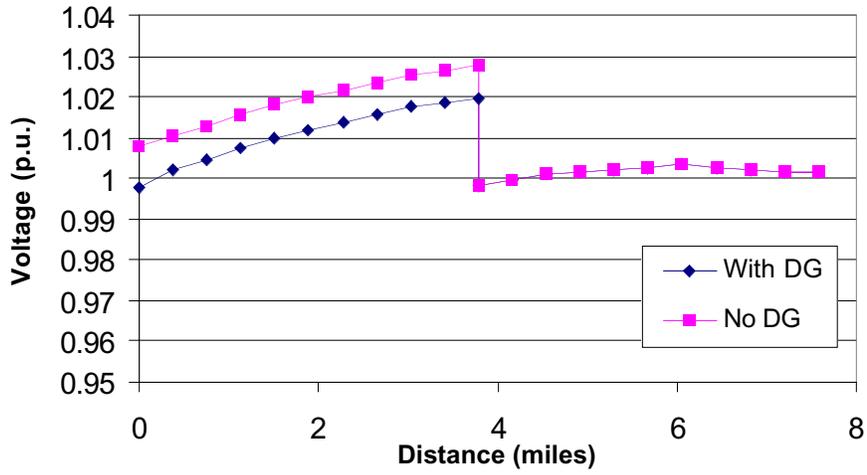
#### Base Case (No DG)



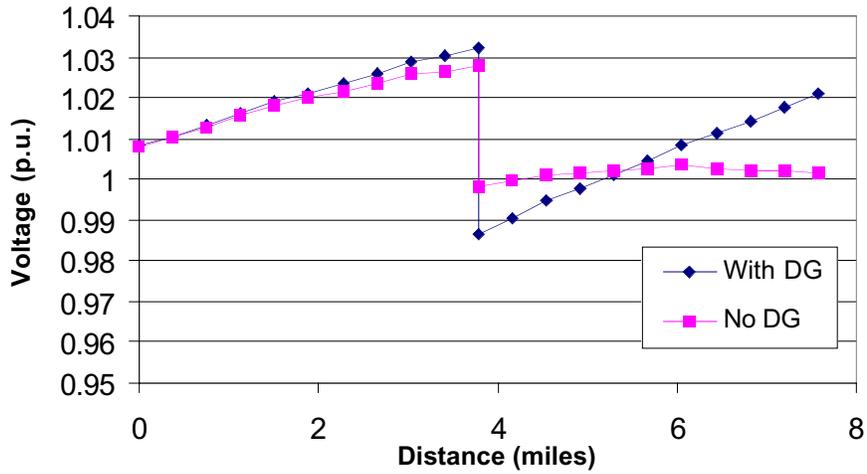
#### Light Load, No Offset, DG at the End (50% Penetration)



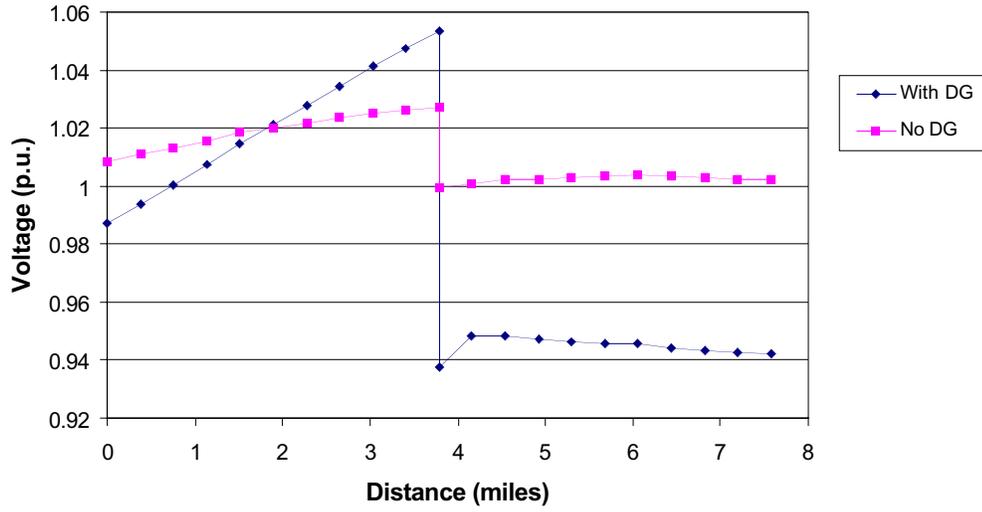
Light Load, No Offset, DG at the Beginning (50% Penetration)



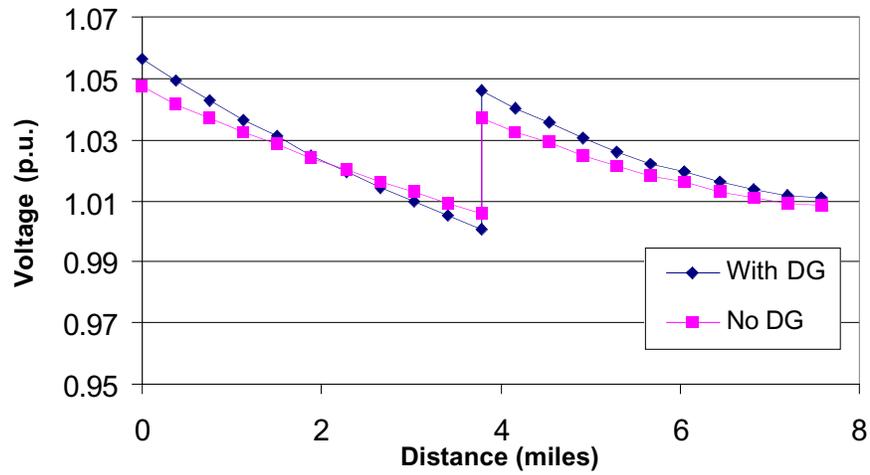
Light Load, Offset Increase, Regulation, DG at the End (100% Penetration)



Light Load, Offset Increase, Regulation, DG at the Beginning, 100%



Heavy Load, Offset Increase, DG Distributed (30% Penetration)



## CASE 3.2

### Description of the Feeder

**Feeder Length:** 8 miles

**LTC: Tap setting** = 1.03, Resistive LDC = 0.25, Reactive LDC = 0.5 (Max = 1.05)

**SVR: Tap setting** = 1.03, Resistive LDC = 0.6, Reactive LDC = 1.1 (Max = 1.05)

**Capacitor Banks:** 900 kVA banks located at 20%, 40%, 60% and 80% of the feeder length.

**Regulation Reference Point (when regulation is enabled):** DG voltage (secondary)

### Scenario 1- Feeder load independent of DG penetration

At light load there is an over-voltage problem for almost all locations of the DG and at low penetration factors. Thresholds of concern are: 20% for DG at the feeder end and middle, and 30% for DG distributed uniformly. Only for DG located at the beginning of the feeder is there no overvoltage situation. The overvoltages occur right before the SVR. For DG at the end, there is also a substantial overvoltage at the feeder end. Regulation by the DG eliminates the problem when the DG is located at the end and is distributed, but regulation does not eliminate overvoltage for DG located at the middle. This is because, for DG at the middle, the DG location is right after the SVR where the overvoltage has already been corrected. Thus, the DG voltage regulator does not observe the overvoltage condition experienced elsewhere.

For heavy load, there is no significant problem, other than a slight overvoltage at high penetration (100%) when the DG is at the end of the feeder.

### Scenario 2 — Peak feeder load increased by an amount equivalent to DG capacity

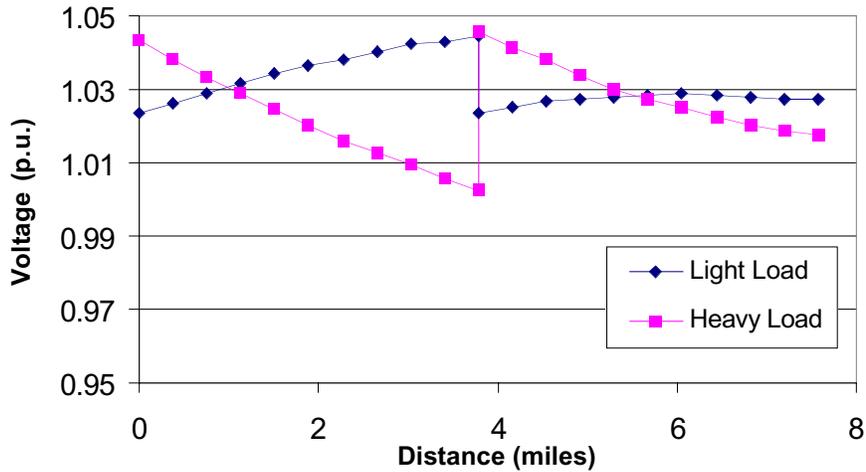
For the light load case, overvoltages also occur in this scenario, but their severity is somewhat reduced by the additional load present. The threshold penetrations where voltage regulation problems begin are somewhat higher (30% for end and middle and 50% for distributed, no problem for DG at the beginning). For this case, DG voltage regulation eliminates the overvoltage for all situations. The reason that the regulation is effective in this scenario is because the voltage at the DG location is more than 1.0 p.u. (which is the DG voltage regulator setpoint assumed in this study), which will cause the DG to absorb reactive power. In contrast, the voltage at the DG location in Scenario 1 is less than 1.0 p.u., the DG's reactive output acts to oppose the system goal of reducing the voltage.

At heavy load, there is undervoltage problem for every location of the DG. When the DG is located at the end, middle or it is distributed, undervoltage occurs only for very high penetration factors (threshold of concern are between 50% and 100%). Only for DG

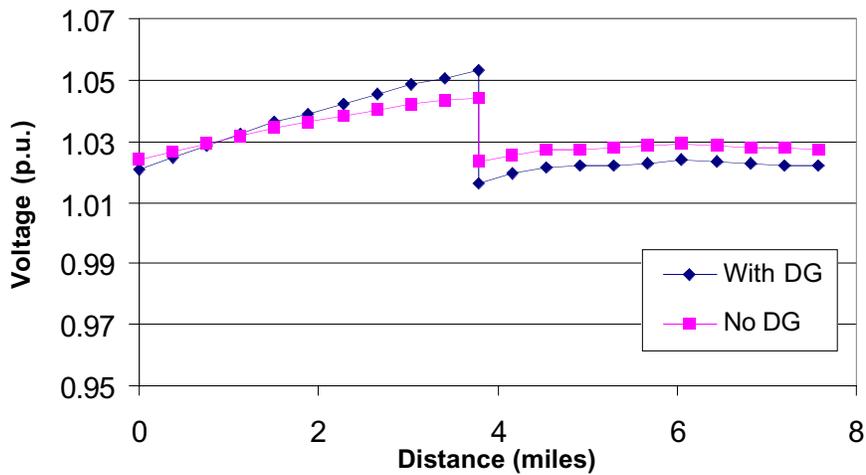
located at the beginning of the feeder is the penetration threshold lower (30%). The undervoltage occurs due to the excessive drops across the feeder starting from the substation, due to the incremental load needed to be supplied. As expected, the worst situation is when the DG is at the beginning since the current in the feeder is the largest, increasing the drops. Regulation by the DG increases the undervoltage problem.

CASE 3.2

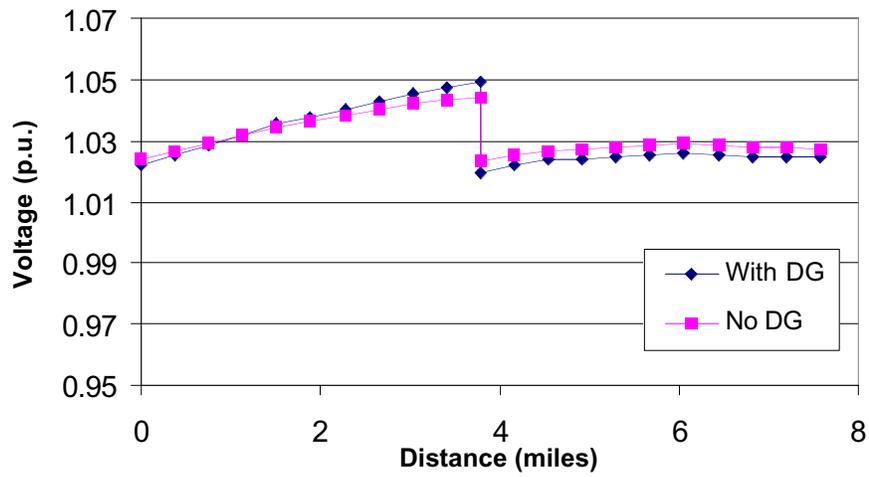
Base Case (No DG)



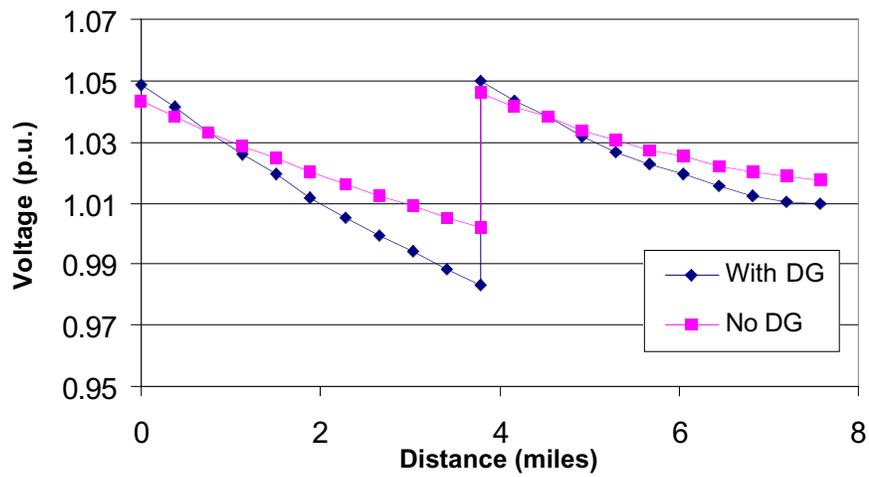
Light Load, No Offset, DG at the Middle (30% Penetration)



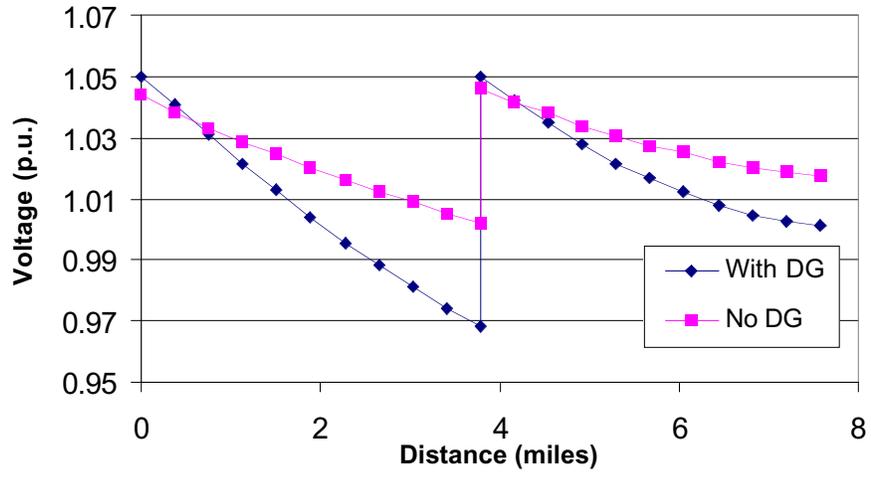
Light Load, No Offset, Regulation, DG at the Middle (30% Penetration)



Heavy Load, Offset Increase, No regulation, DG at the Beginning (30% Penetration)



Heavy Load, Offset Increase, No regulation, DG at the Beginning (50% Penetration)



## CASE 3.3

### Description of the Feeder

**Feeder Length:** 8 miles

**LTC: Tap setting** = 1.03, Resistive LDC =0.25, Reactive LDC = 0.5 (Max =1.05)

**SVR: Tap setting** = 1.03, Resistive LDC =0.6, Reactive LDC = 1.1 (Max= 1.05)

**Capacitor Banks:** 900 kVA banks located at 20%, 40%, 60% and 80% of the feeder length.

**Regulation Reference Point (when regulation is enabled):** Bus Voltage (primary)

#### Scenario 1- Feeder load independent of DG penetration

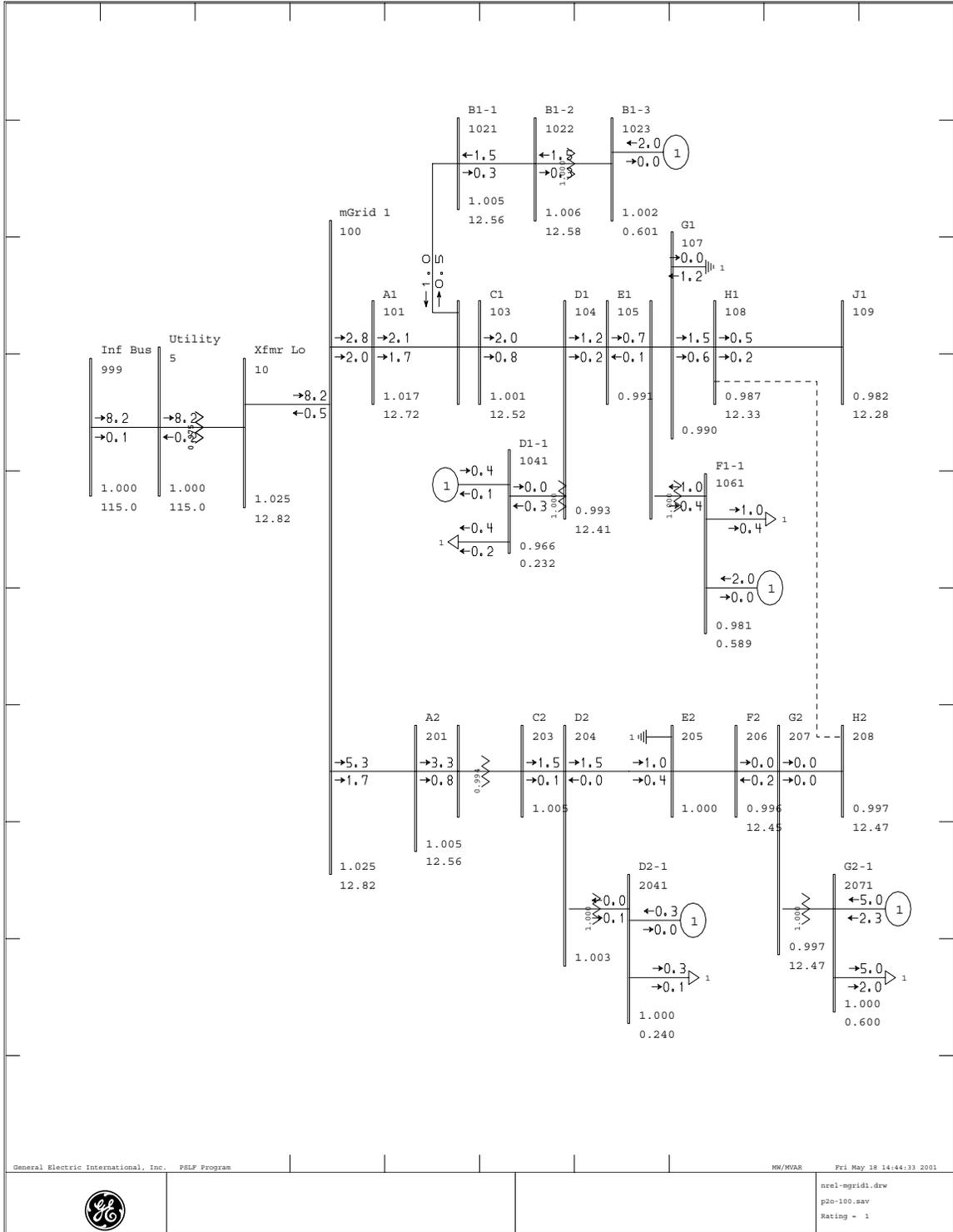
This case differs from Case 3.2 in that the DG voltage regulation seeks to regulate the primary voltage at the DG location instead of the secondary voltage. The results for this scenario are very similar for those of Case 3.2.

#### Scenario 2 — Peak feeder load increased by an amount equivalent to DG capacity

The voltage at the primary side of the distribution transformer is usually larger than the per-unit voltage at the secondary (DG) side for this situation. The voltage difference, however, is small - usually half a percent, so the regulation performance is very similar. For the light load case, similar to Case 3.2 where the secondary (DG) voltage was regulated, the overvoltage is eliminated. Regulation of the primary side for the heavy load case does not remedy the undervoltage problem and can actually aggravate the problem.

# Appendix C. P2 Case Study Voltage Profiles

One-line Diagram Showing Voltages, Active and Reactive Flows  
At 100% of base load



General Electric International, Inc. PSLF Program

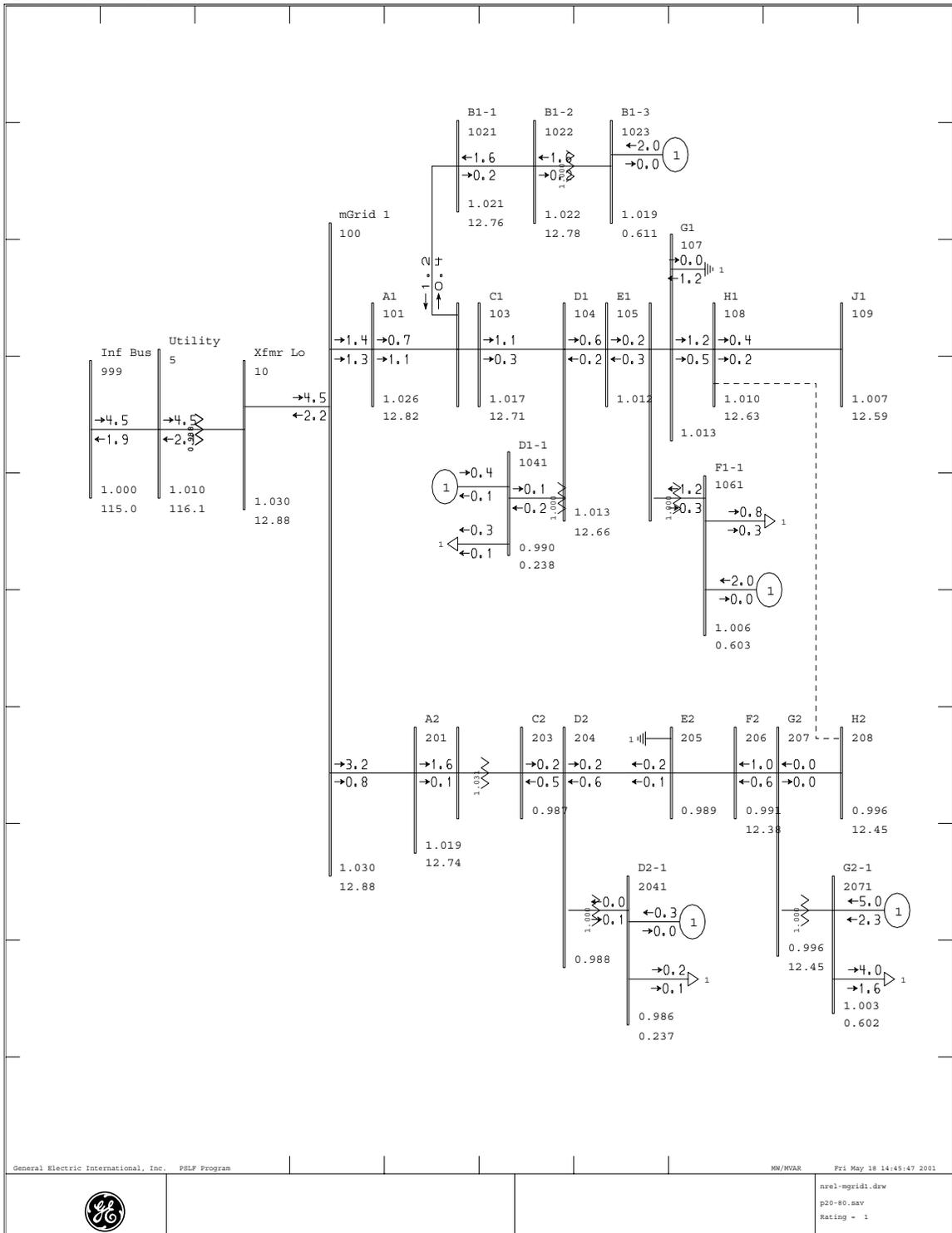
NW/WPAR

Fri May 18 14:44:33 2001

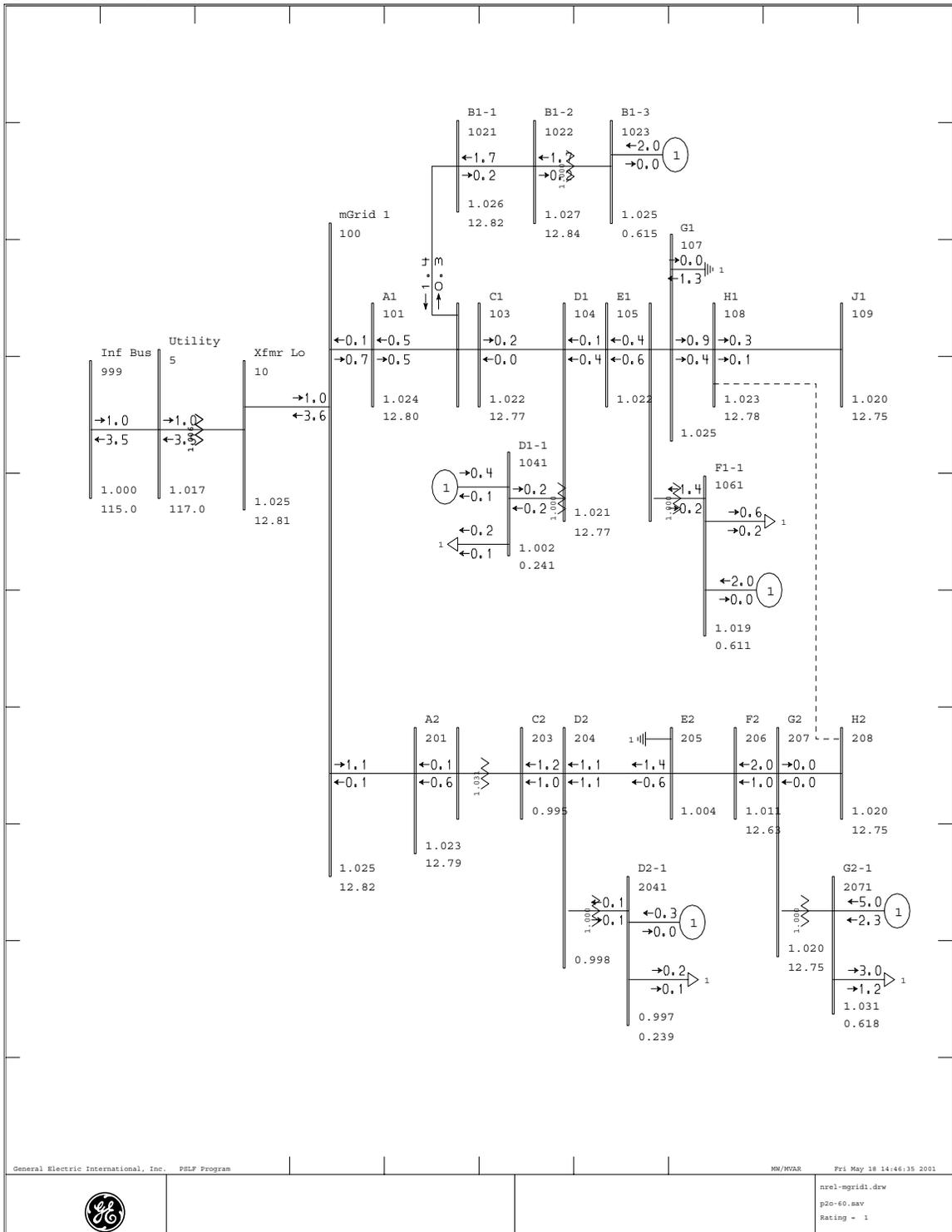


nrel-mgrid1.drw  
p2o-100.sav  
Rating - 1

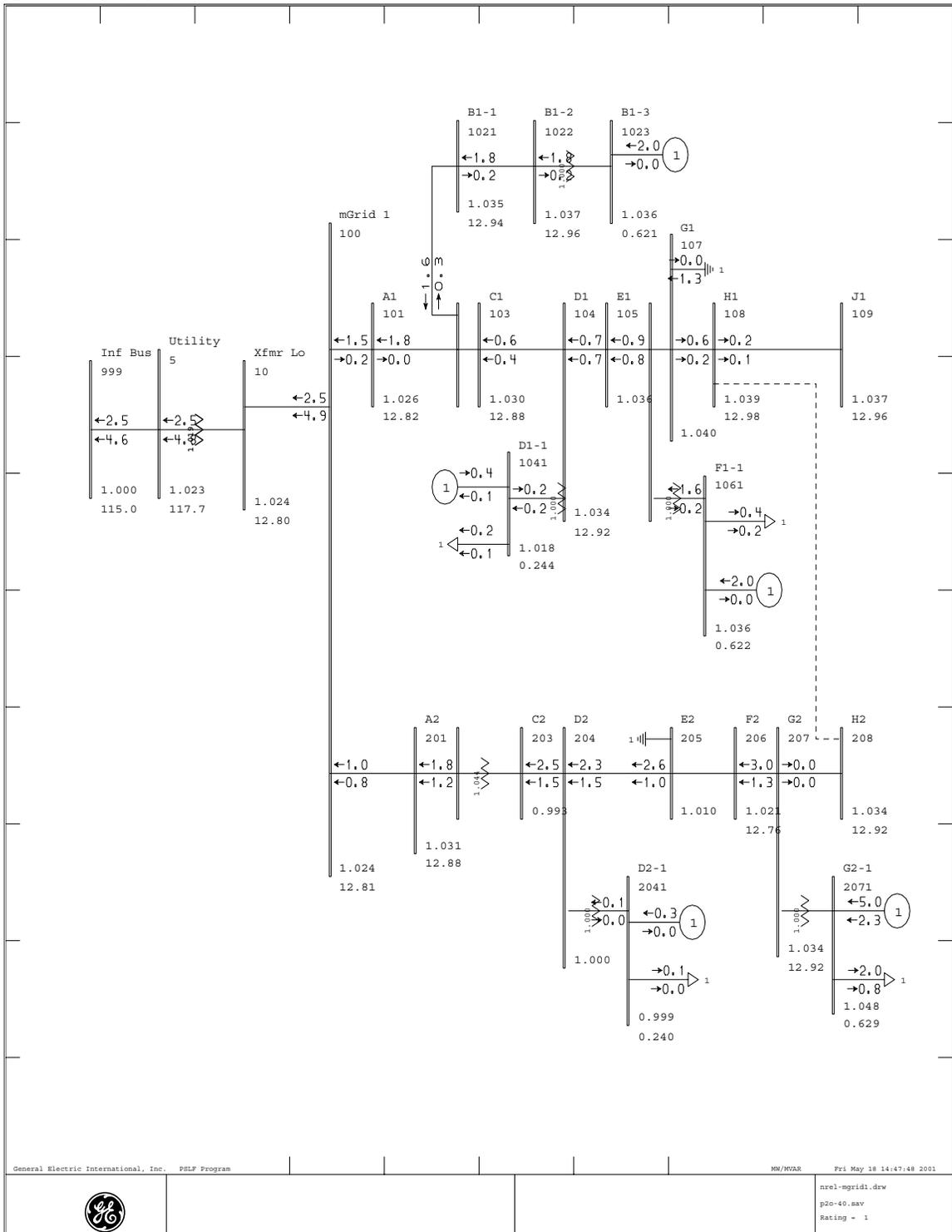
One-line Diagram Showing Voltages, Active and Reactive Flows  
At 80% of base load



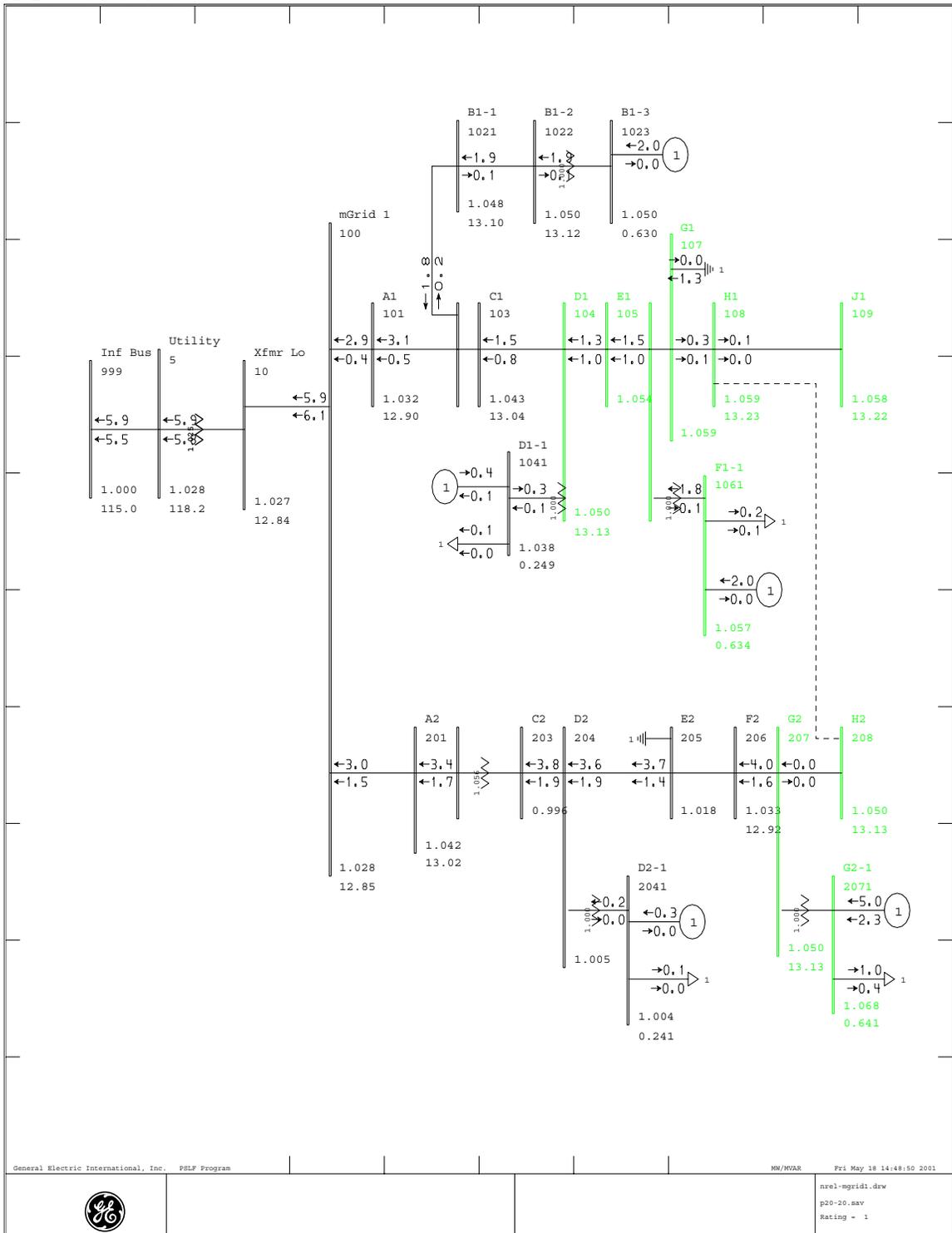
One-line Diagram Showing Voltages, Active and Reactive Flows  
At 60% of base load



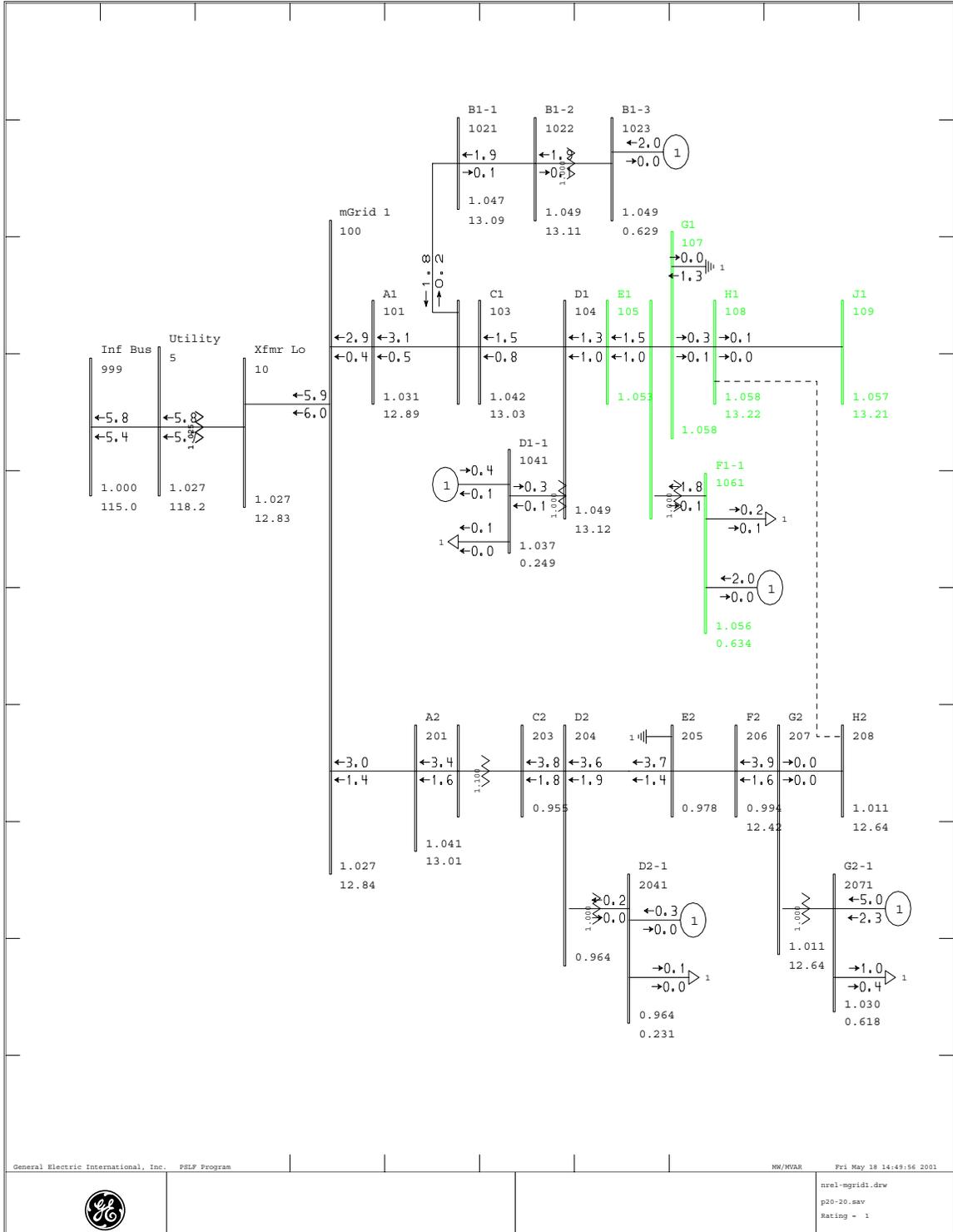
One-line Diagram Showing Voltages, Active and Reactive Flows  
At 40% of base load



One-line Diagram Showing Voltages, Active and Reactive Flows  
At 20% of base load



One-line Diagram Showing Voltages, Active and Reactive Flows  
 At 20% of base load  
 With SVR control reversal due feeder active flow reversal



General Electric International, Inc. PELF Program

NW/MVAR

Fri May 18 14:49:56 2001



nrel-mgrid1.dwg  
 p20-20.sav  
 Rating - 1

# Appendix D. Flicker

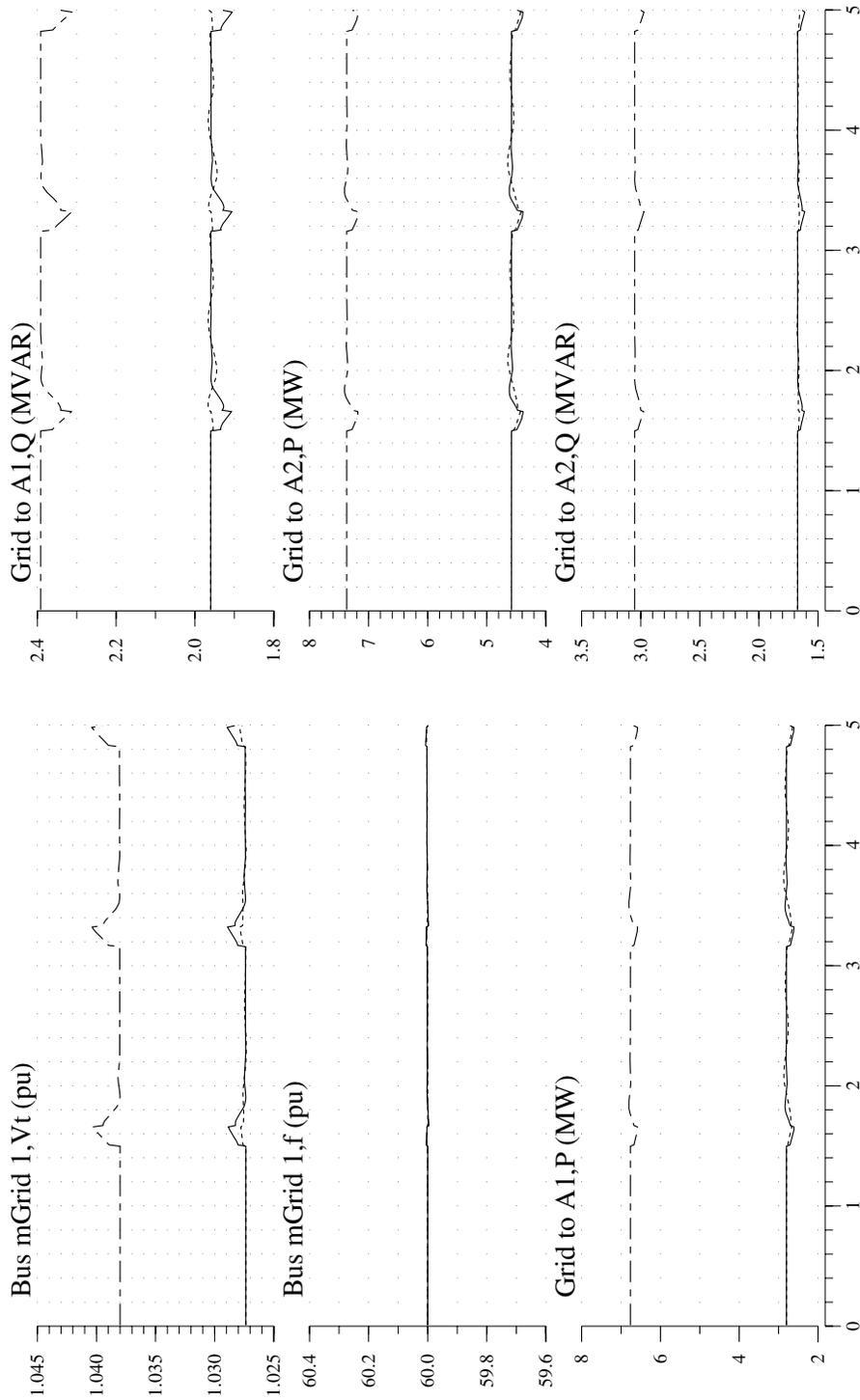
## **SEPARATOR 1: P2 SYSTEM LOAD-INDUCED FLICKER CASE.**

3 Traces: No DGs; with Inverter type DGs; with Rotating type DGs  
Without Voltage Control

# Flicker: Load fluctuations. Without Voltage control

## System Quantities

inverter type DG (—), rotating DG (---), no DG (----

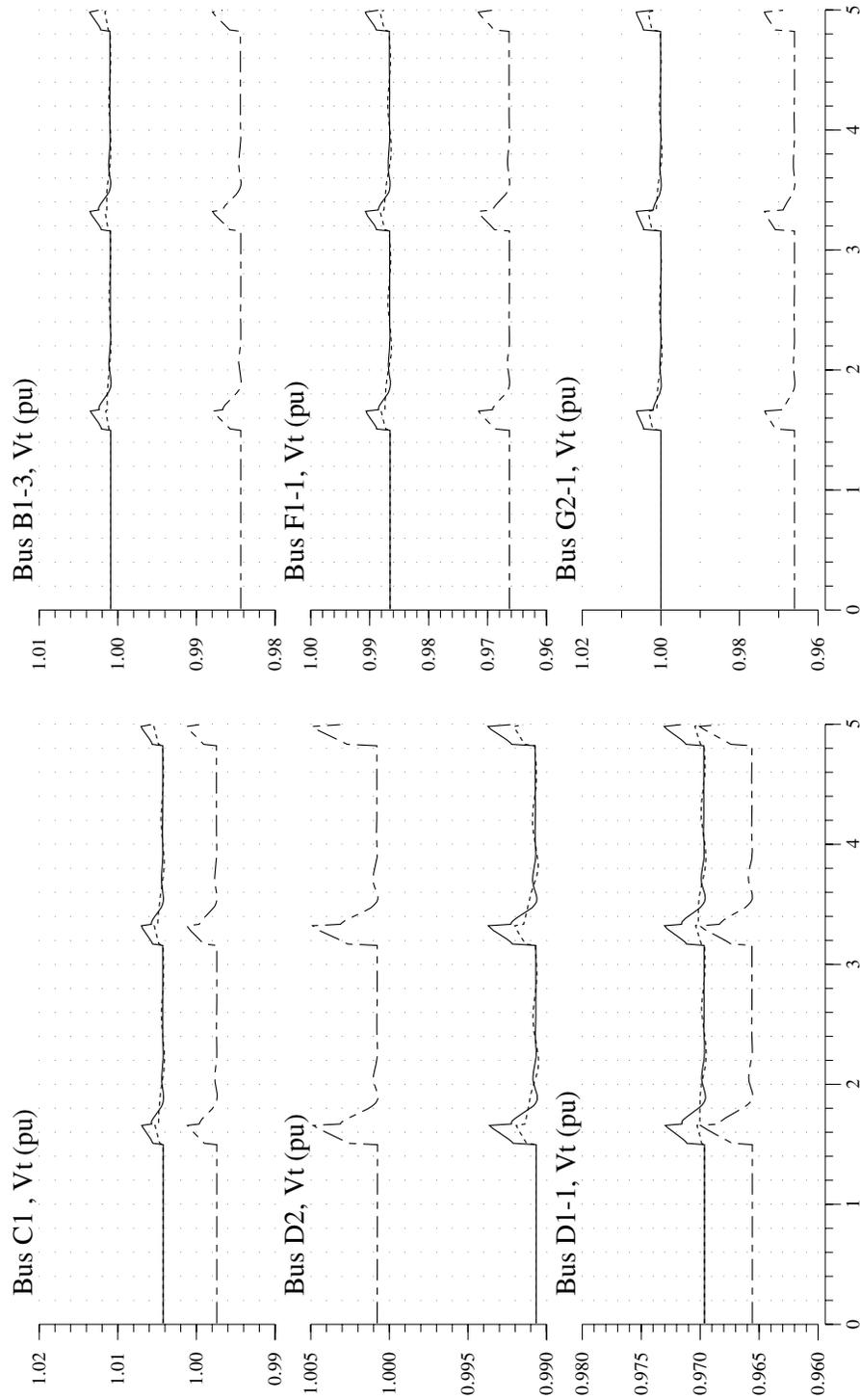


Time (seconds)

# Flicker: Load fluctuations. Without Voltage control

## DG Voltages

inverter type DG (—), rotating DG (---), no DG (---)



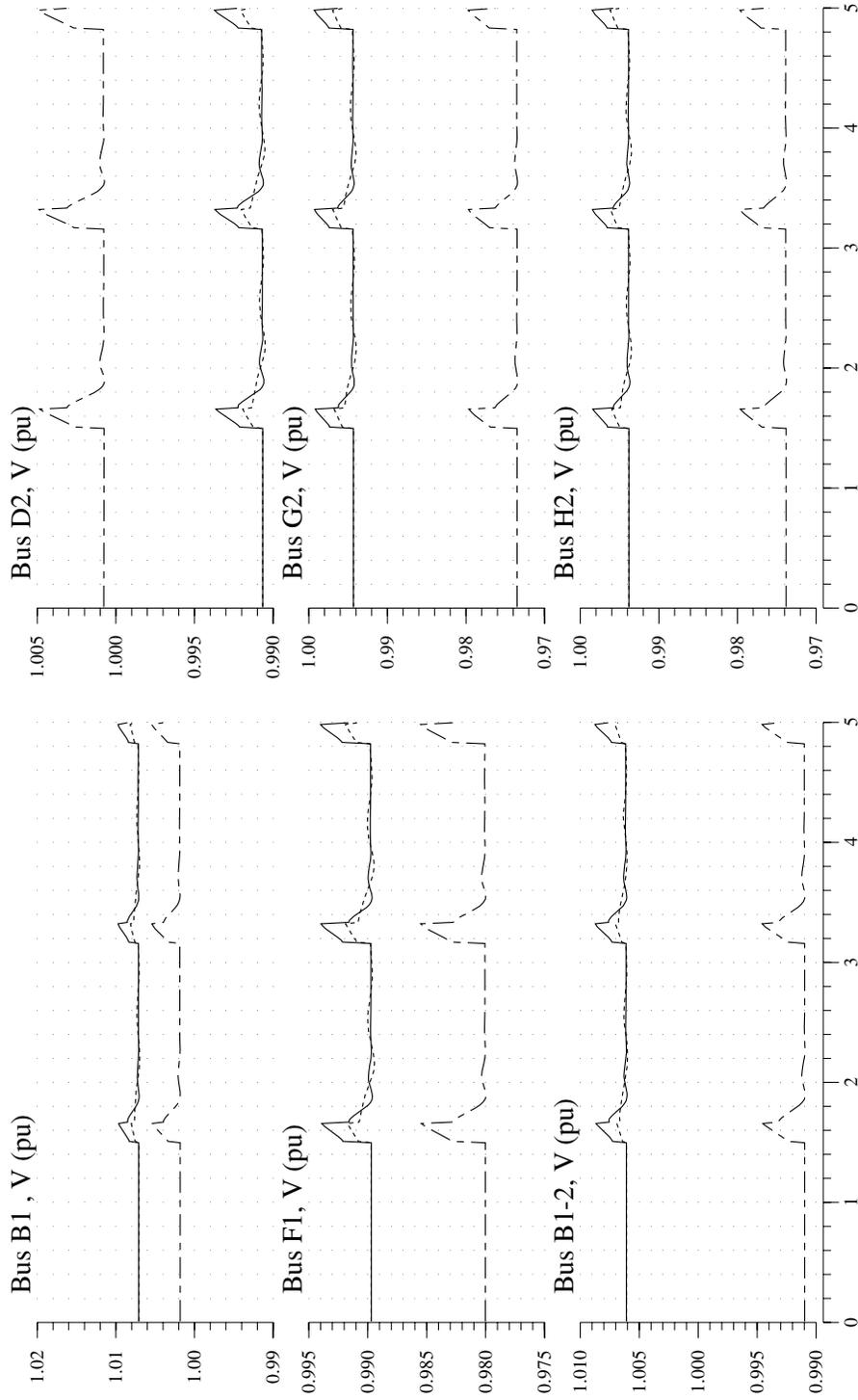
Time (seconds)

Time (seconds)

# Flicker: Load fluctuations. Without Voltage control

## Voltages

inverter type DG (—), rotating DG (---), no DG (---)



Time (seconds)

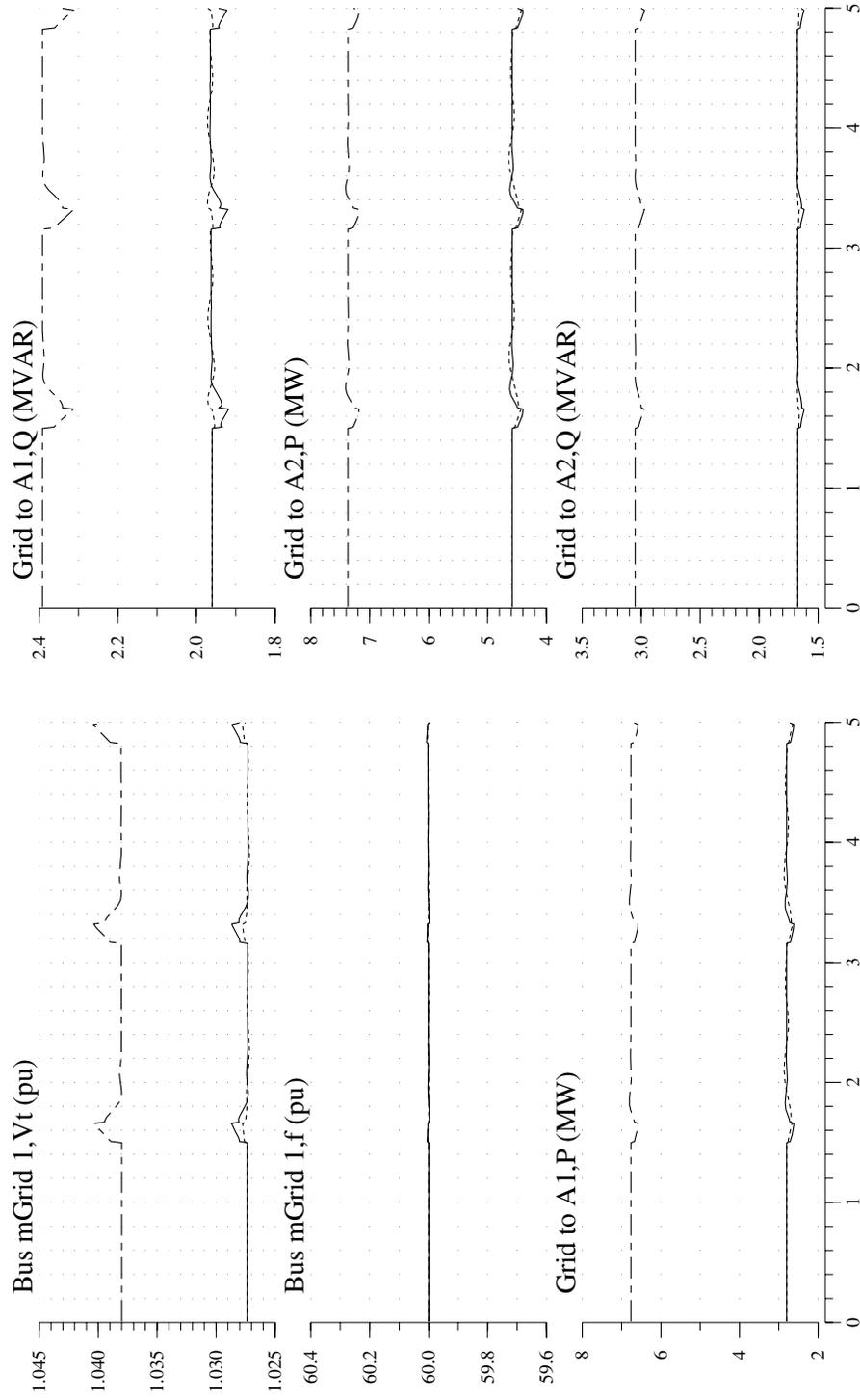
**SEPARATOR 2: P2 SYSTEM LOAD-INDUCED FLICKER CASE.**

3 Traces: No DGs; with Inverter type DGs; with Rotating type DGs  
With Voltage Control

# Flicker: Load fluctuations. Voltage control

## System Quantities

inverter type DG (—), rotating DG (---), no DG (----



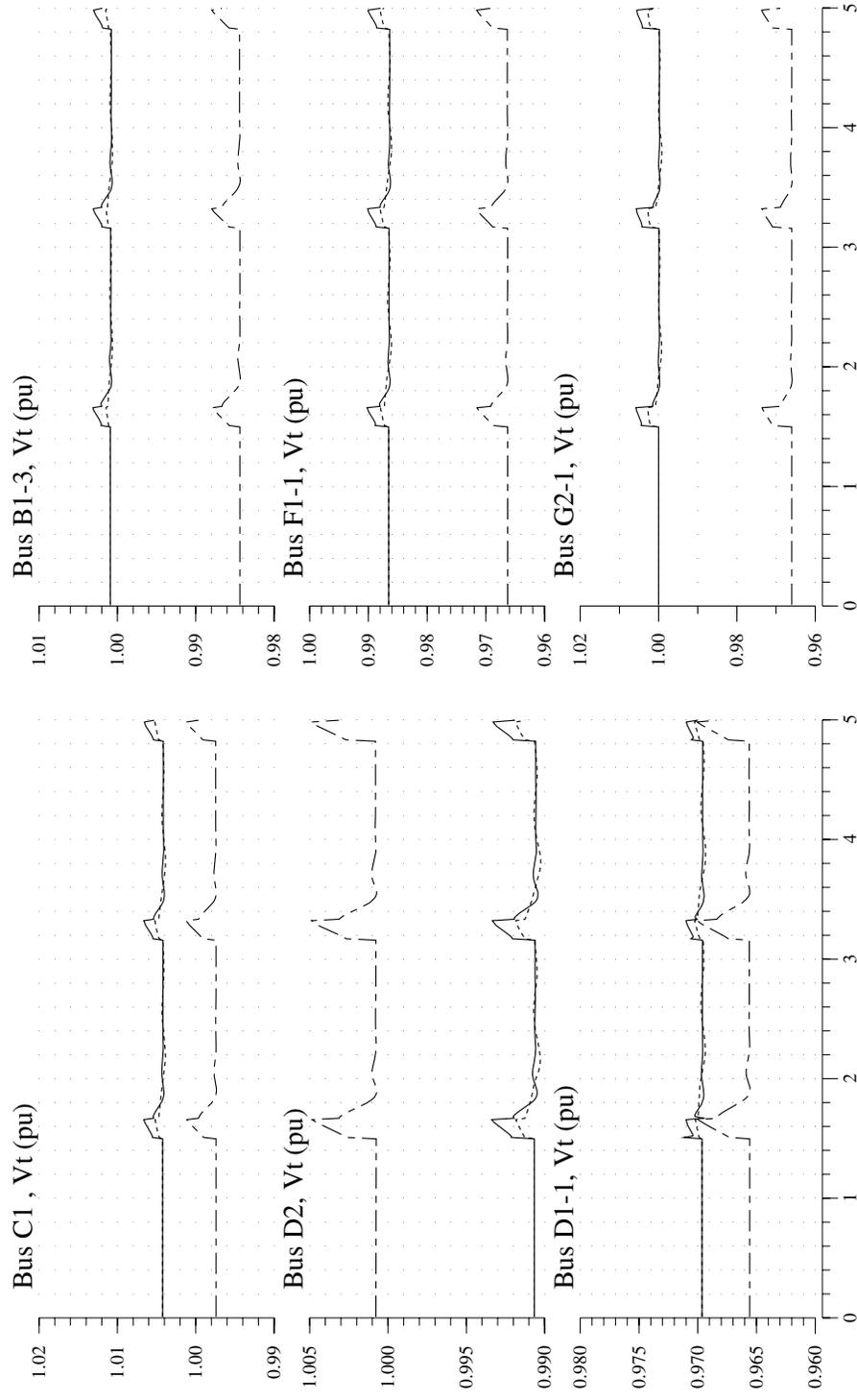
Time (seconds)

Time (seconds)

# Flicker: Load fluctuations. Voltage control

## DG Voltages

inverter type DG (—), rotating DG (---), no DG (---)



Time (seconds)

22-JUN-2001 17:16:18 out\psfiles\loadffi-inv-v.chan

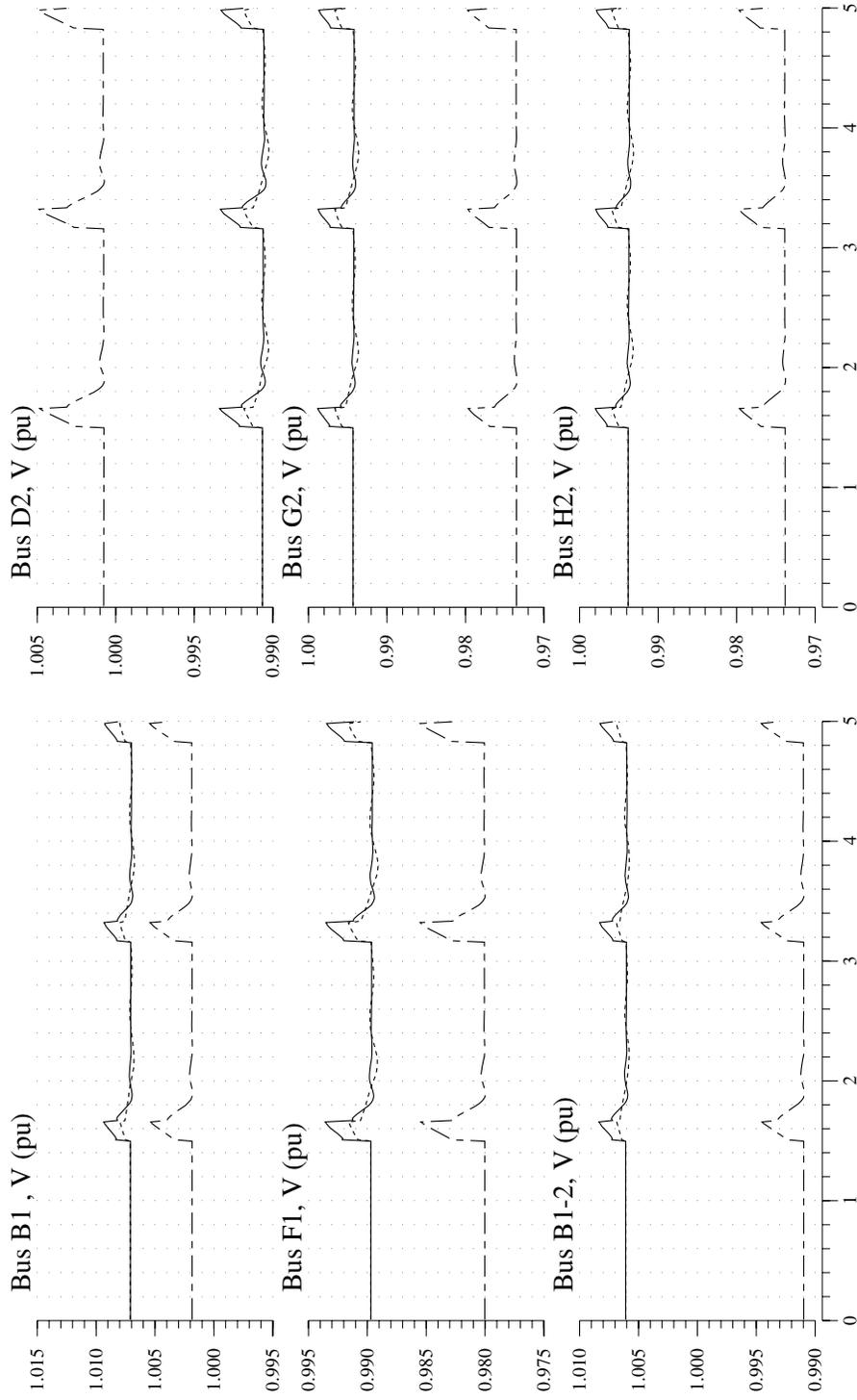
Time (seconds)

Page 2

# Flicker: Load fluctuations. Voltage control

Voltages

inverter type DG (—), rotating DG (---), no DG (---)



Time (seconds)

---

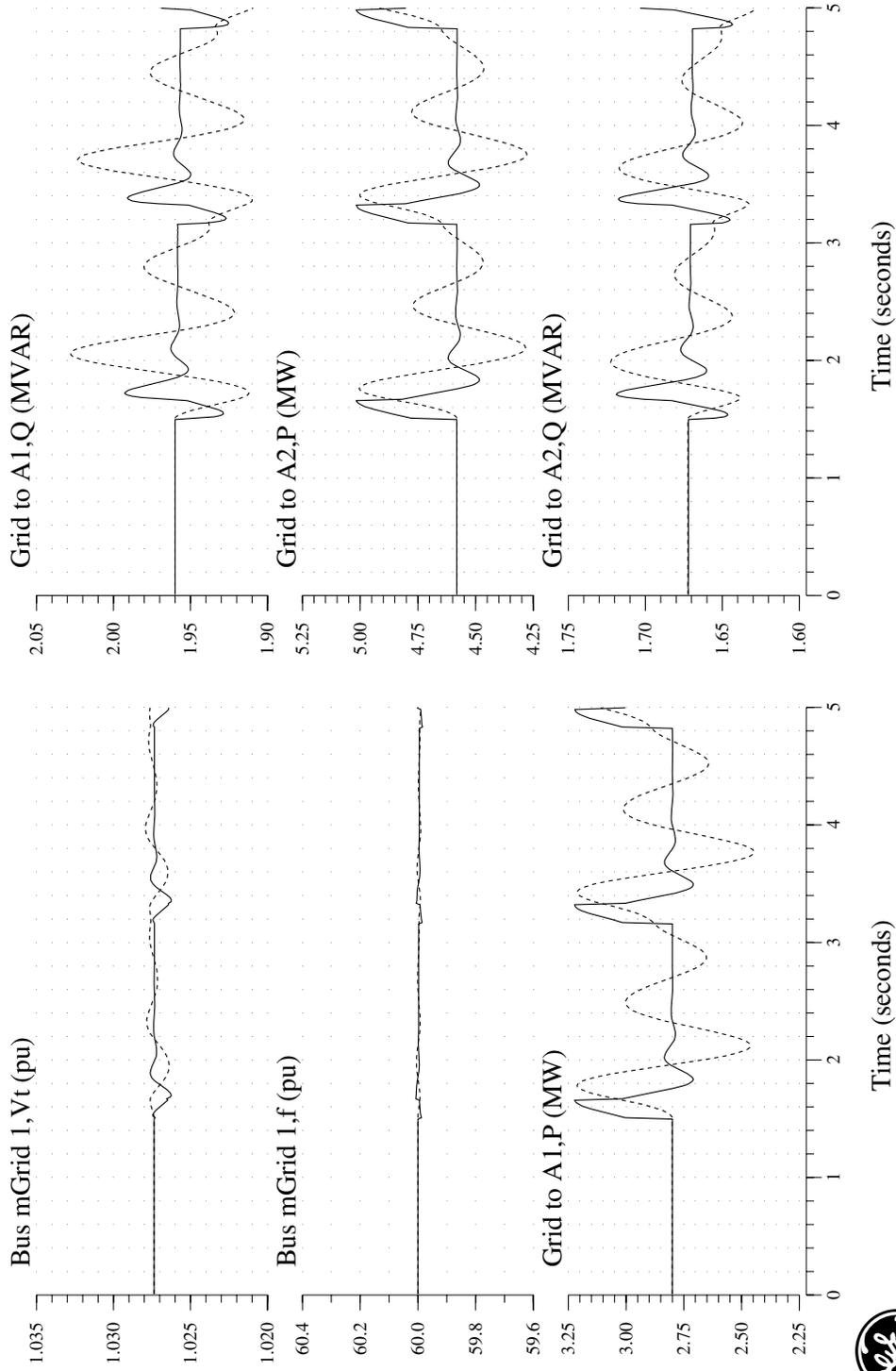
**SEPARATOR 3: P2 SYSTEM DG-INDUCED FLICKER CASE.**

2 Traces: with Inverter type DGs; with Rotating type DGs  
Without Voltage Control

# Flicker: Prime mover fluctuations. Without Voltage control

## System Quantities

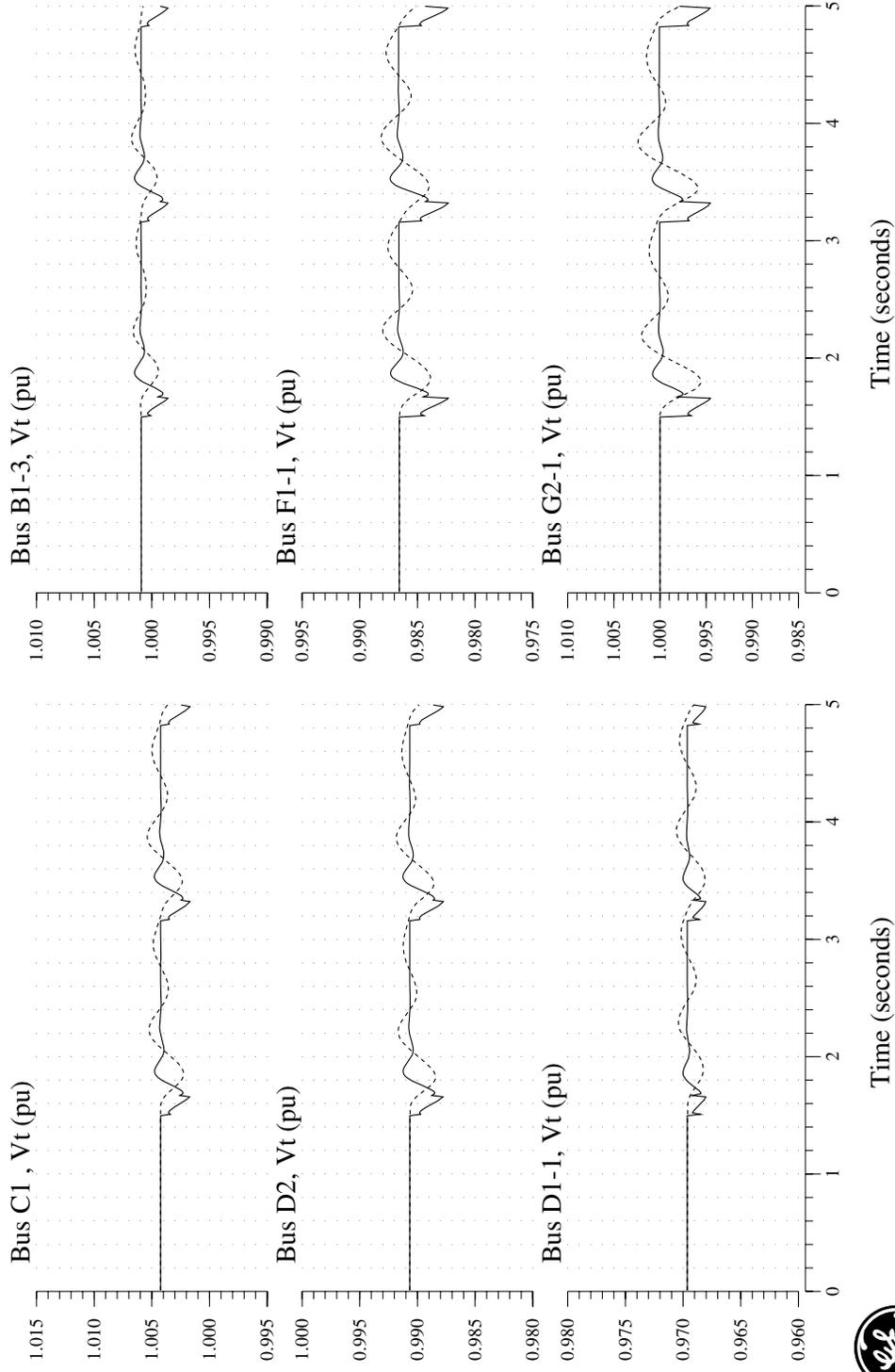
inverter type DG (—), rotating DG (---)



# Flicker: Prime mover fluctuations. Without Voltage control

## DG Voltages

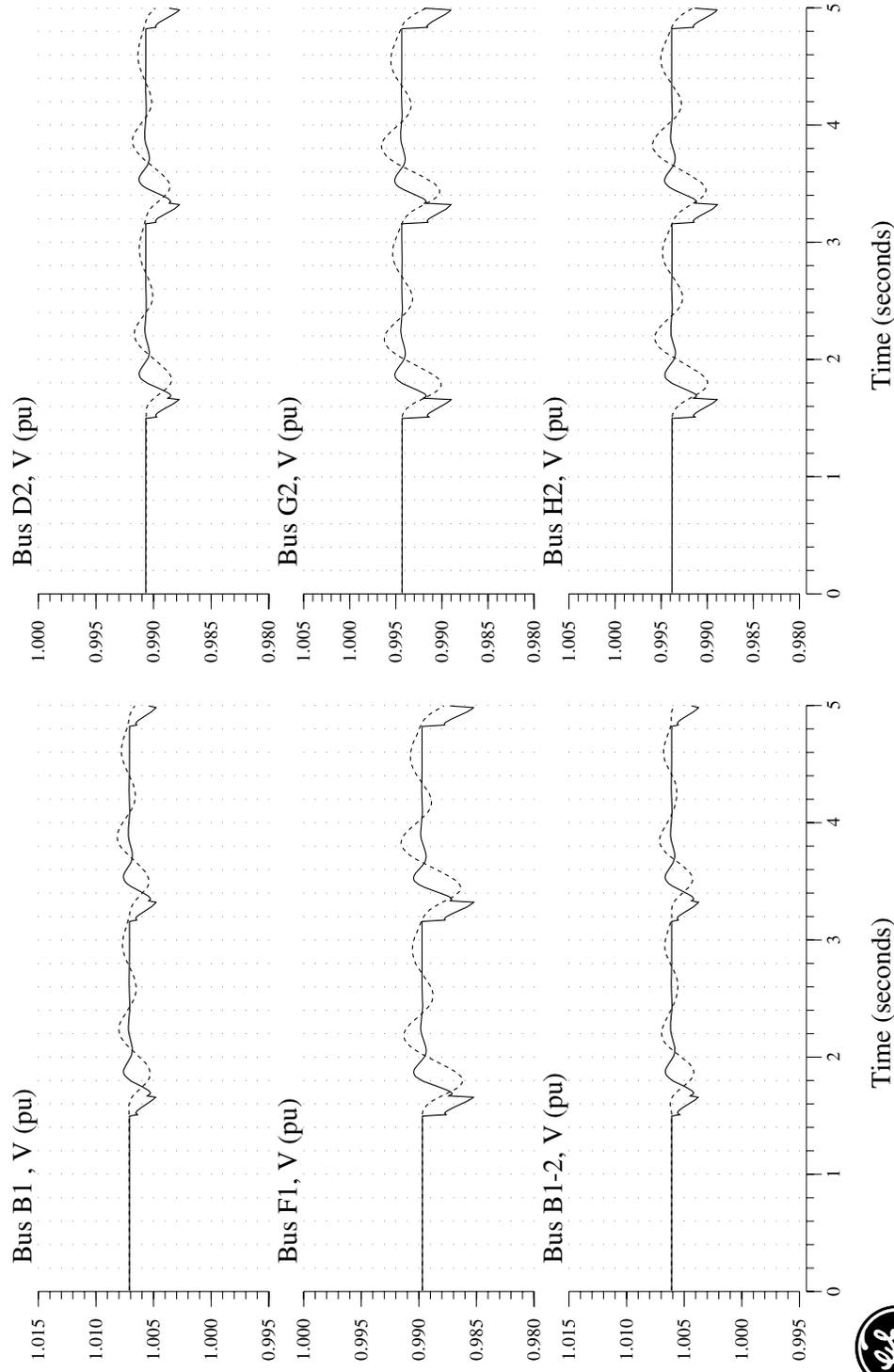
inverter type DG (—), rotating DG (---)



# Flicker: Prime mover fluctuations. Without Voltage control

## Voltages

inverter type DG (—), rotating DG (- - -)



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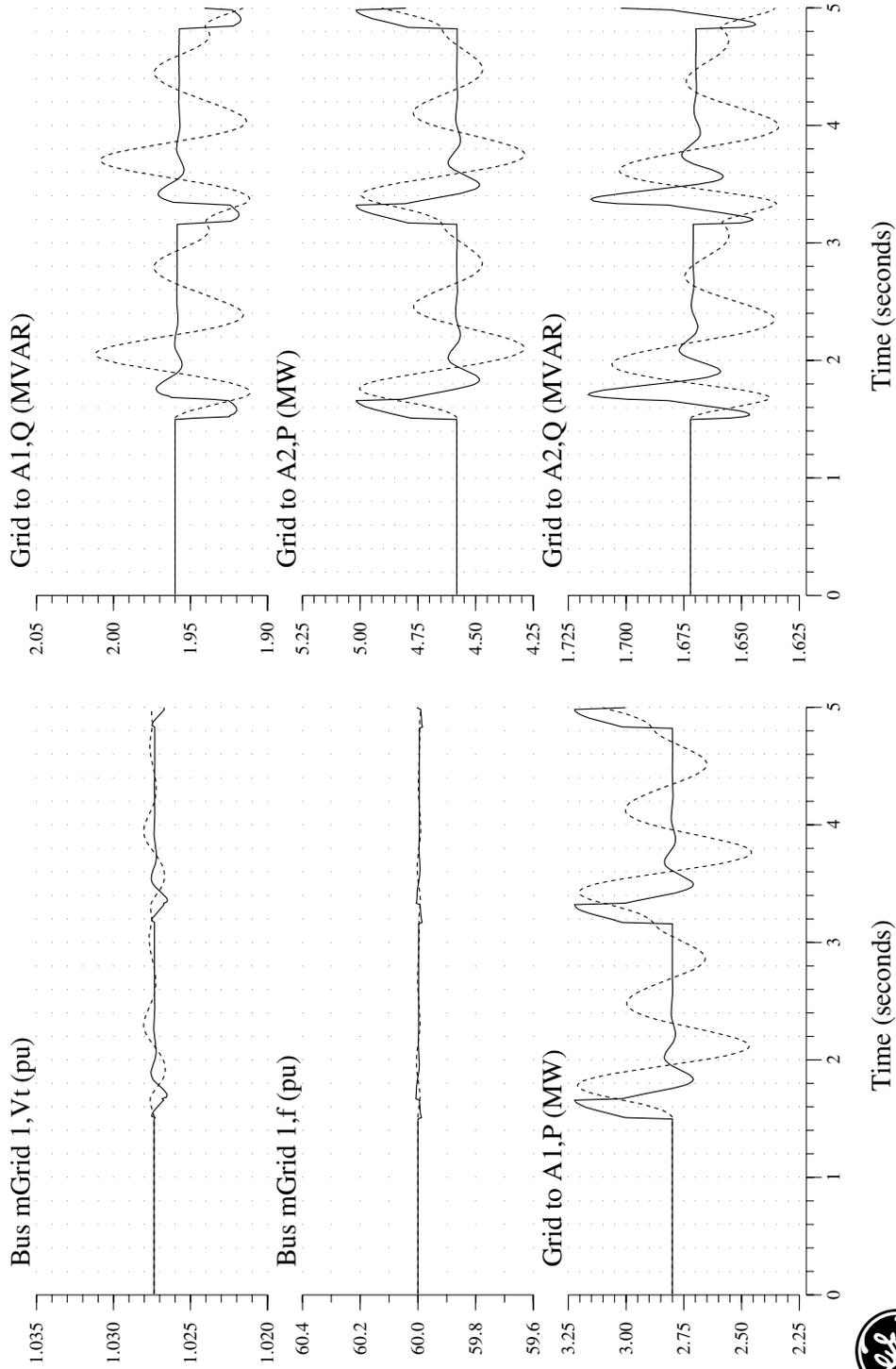
**SEPARATOR 4: P2 SYSTEM DG-INDUCED FLICKER CASE.**

2 Traces: with Inverter type DGs; with Rotating type DGs  
With Voltage Control

# Flicker: Prime mover fluctuations. Voltage control

## System Quantities

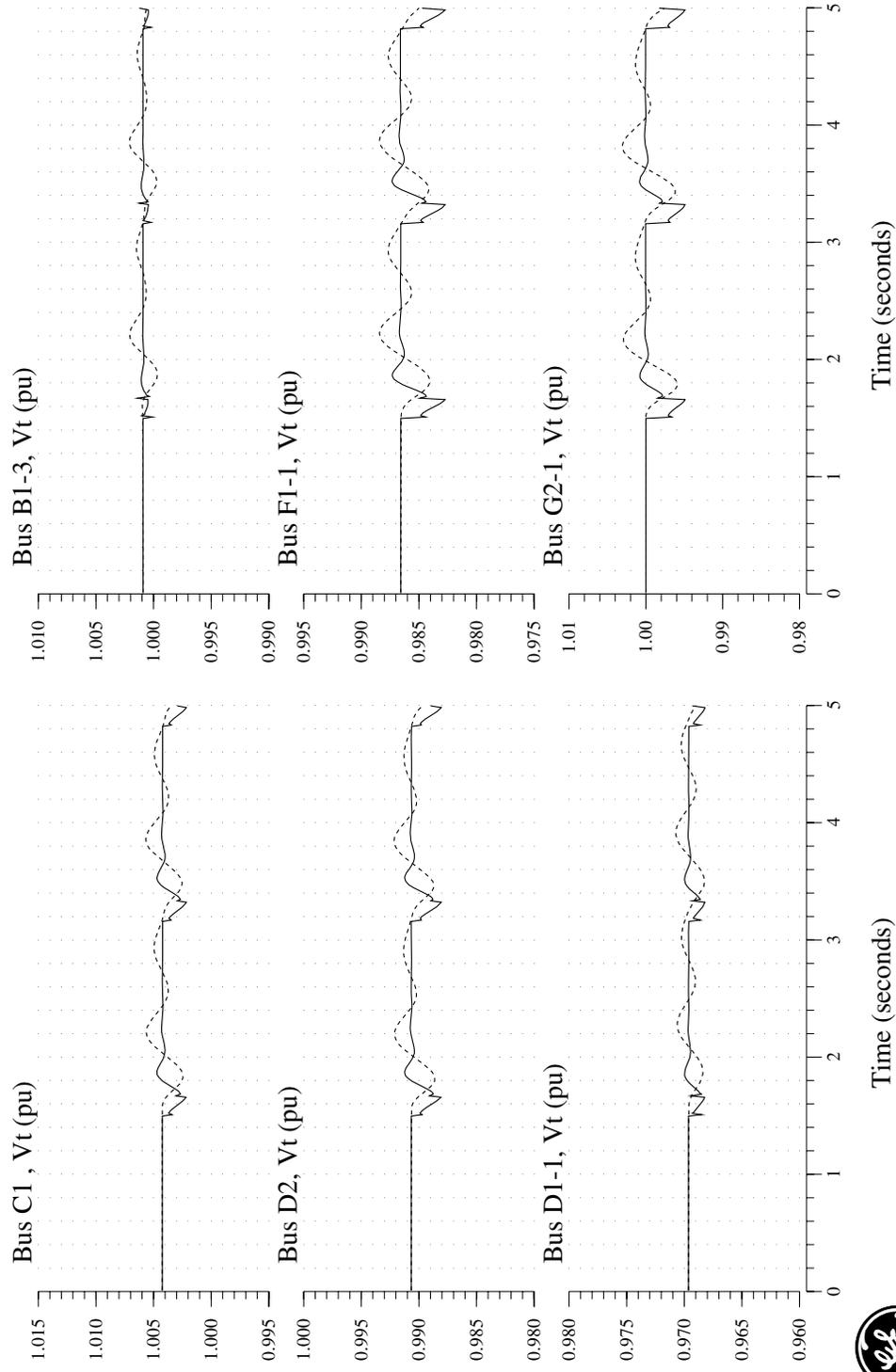
inverter type DG (—), rotating DG (- - -)



# Flicker: Prime mover fluctuations. Voltage control

## DG Voltages

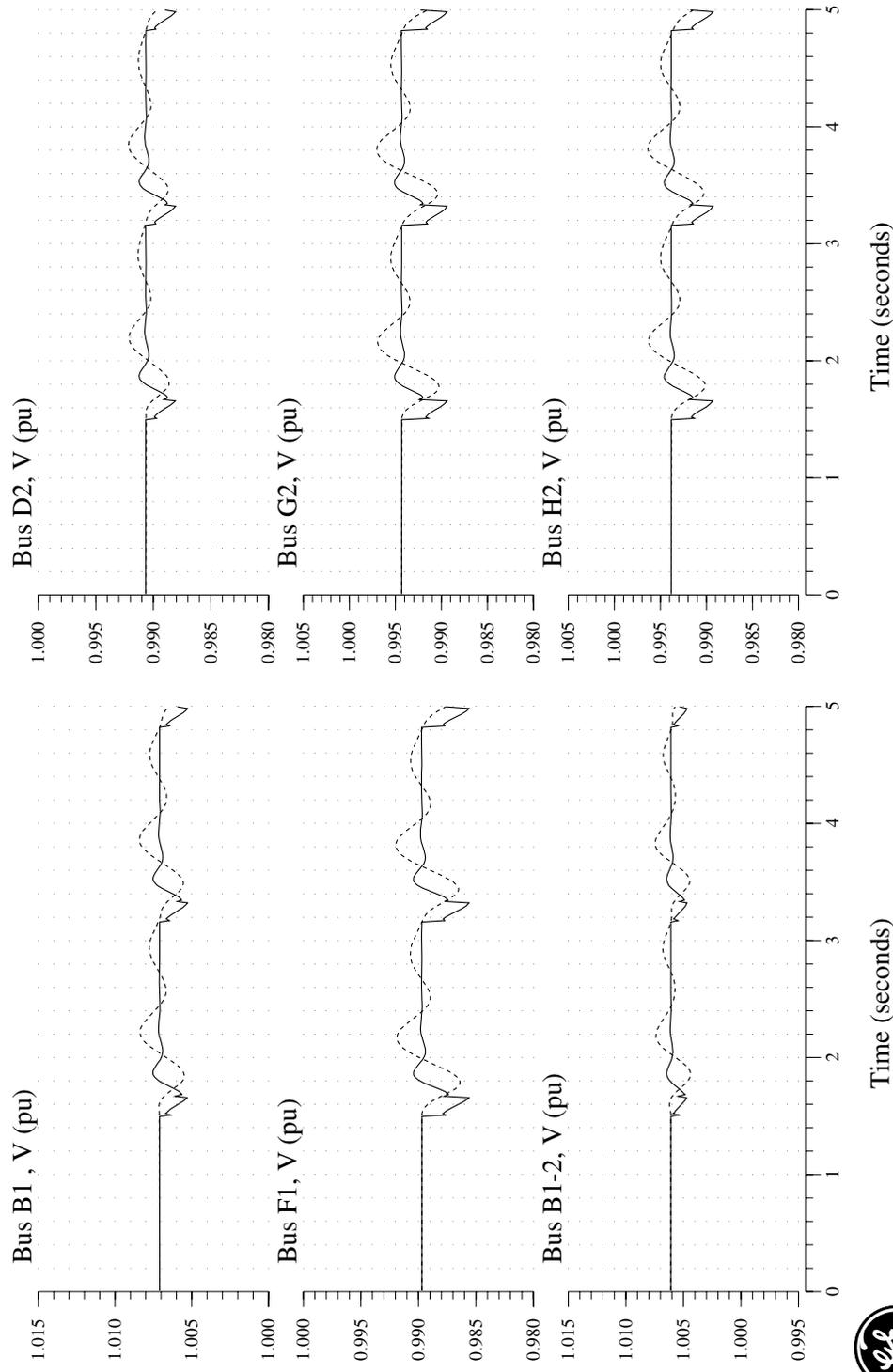
inverter type DG (—), rotating DG (- - -)



# Flicker: Prime mover fluctuations. Voltage control

## Voltages

inverter type DG (—), rotating DG (- - -)



# Appendix E.

## Sequence Circuit During a Single-Phase Fault

During a single-phase fault, for example, phase A to ground fault, the fault voltage and currents are:

$$V_{A,fault} = 0 \quad (1)$$

$$I_{B,fault} = I_{C,fault} = 0 \quad (2)$$

Convert the equations using symmetrical components, one can obtain:

$$V_{1,A} + V_{2,A} + V_{0,A} = 0 \quad (3)$$

$$a^2 \cdot I_{1,A} + a \cdot I_{1,A} + I_{1,A} = a \cdot I_{1,A} + a^2 \cdot I_{1,A} + I_{1,A} = 0 \quad (4)$$

note that:

$$\begin{bmatrix} F_A \\ F_B \\ F_C \end{bmatrix} = \begin{bmatrix} 1 & 1 & 1 \\ a^2 & a & 1 \\ a & a^2 & 1 \end{bmatrix} \cdot \begin{bmatrix} F_1 \\ F_2 \\ F_0 \end{bmatrix}, \quad (5)$$

where:  $F_{A,B,C}$  is phase voltage or current,  $F_{1,2,0}$  is sequence voltage or current.

From (4), the sequence current relationship can be derived

$$I_{1,A} = I_{2,A} = I_{0,A} \quad (6)$$

Based on (3) and (6), Figure 1 shows the positive-, negative- and zero-sequence equivalent circuit after phase A single-phase fault.

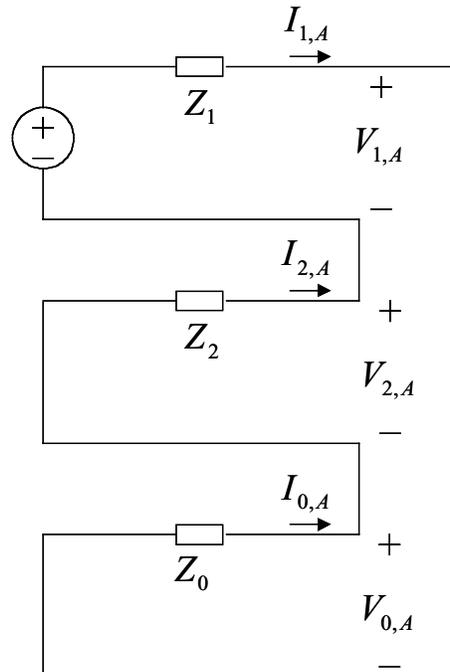


Figure 1 Sequence circuit during a single-phase fault.

Where:  $Z_1$ ,  $Z_2$ , and  $Z_0$  are the overall system positive-, negative- and zero-sequence impedances during the fault.

The sequence voltages  $V_{1,A}$ ,  $V_{2,A}$ , and  $V_{0,A}$  can be calculated based on the circuit in Figure 1.

Then, the unfaulted phase voltages are:

$$V_B = a^2 \cdot V_{1,A} + a \cdot V_{2,A} + V_{0,A}$$

$$V_C = a \cdot V_{1,A} + a^2 \cdot V_{2,A} + V_{0,A}$$

# Appendix F. Local Dynamics

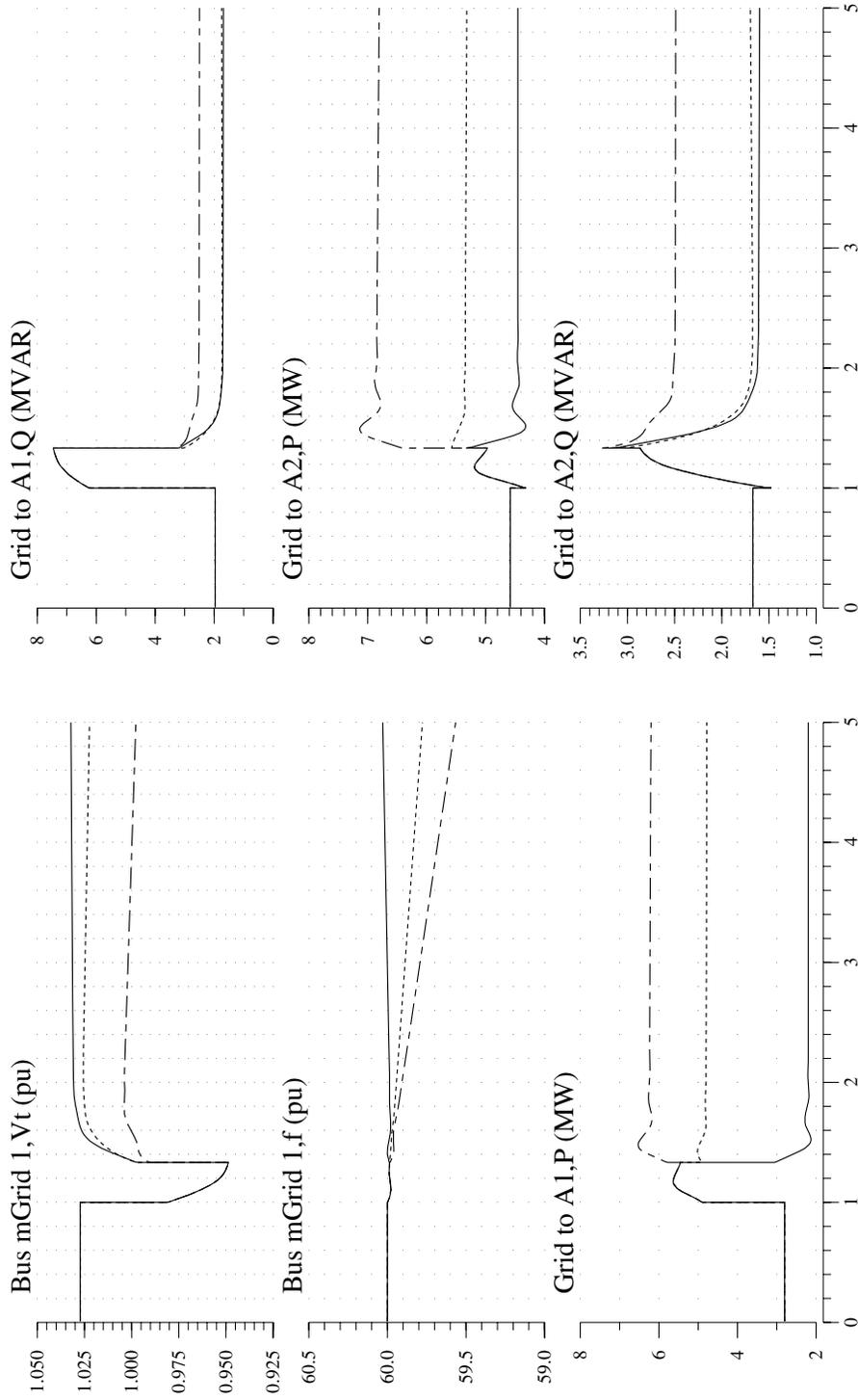
## **SEPARATOR 1: P2 SYSTEM RESPONSE TO A LATERAL FAULT**

All inverter-based DGs with no special controls (constant current control)

# System 2: Without Controls

## System Quantities

no DG trip (—), 3DG trip (---), all DG trip (---)



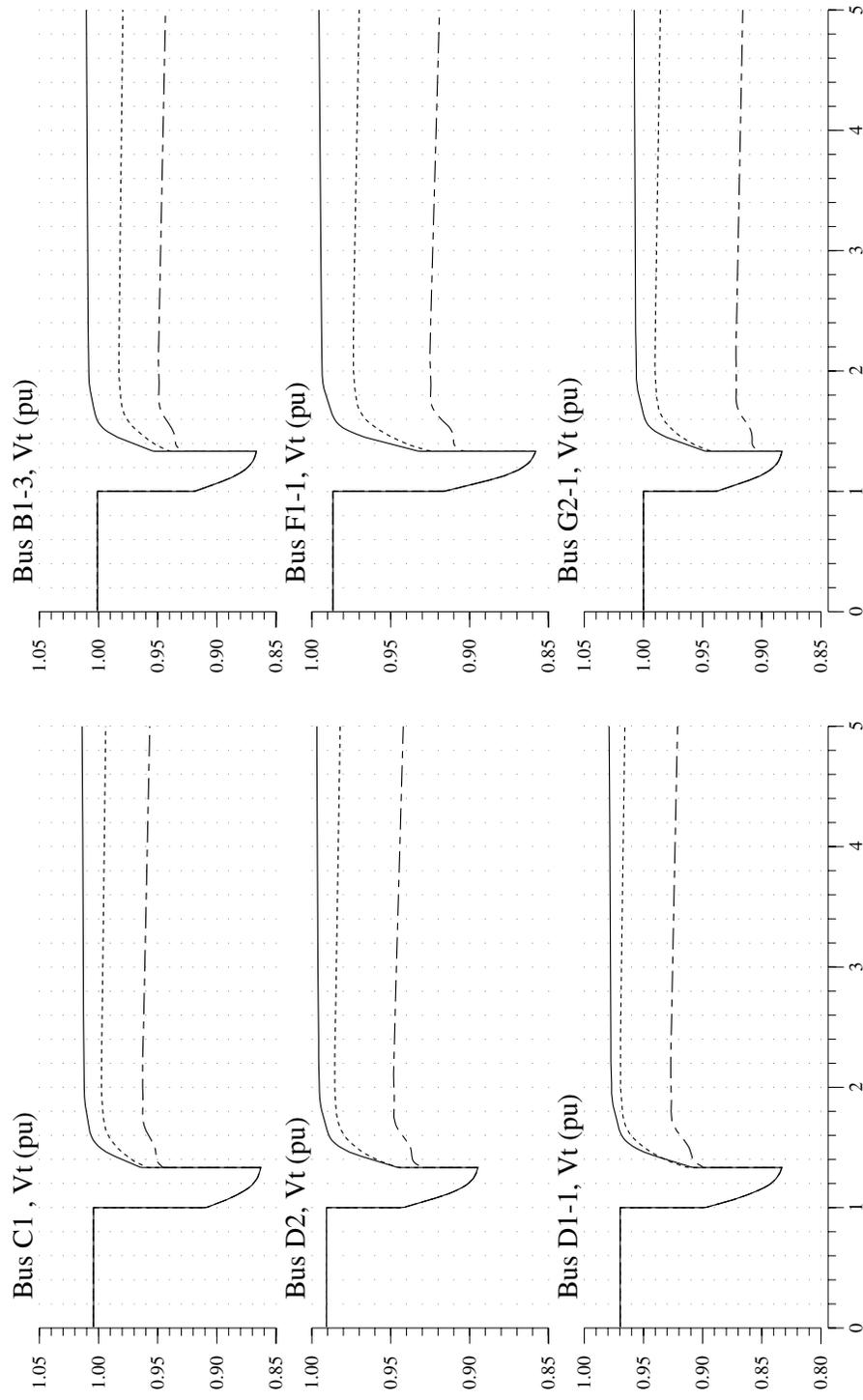
Time (seconds)

Time (seconds)

# System 2: Without Controls

## Voltages

no DG trip (—), 3DG trip (---), all DG trip (---)



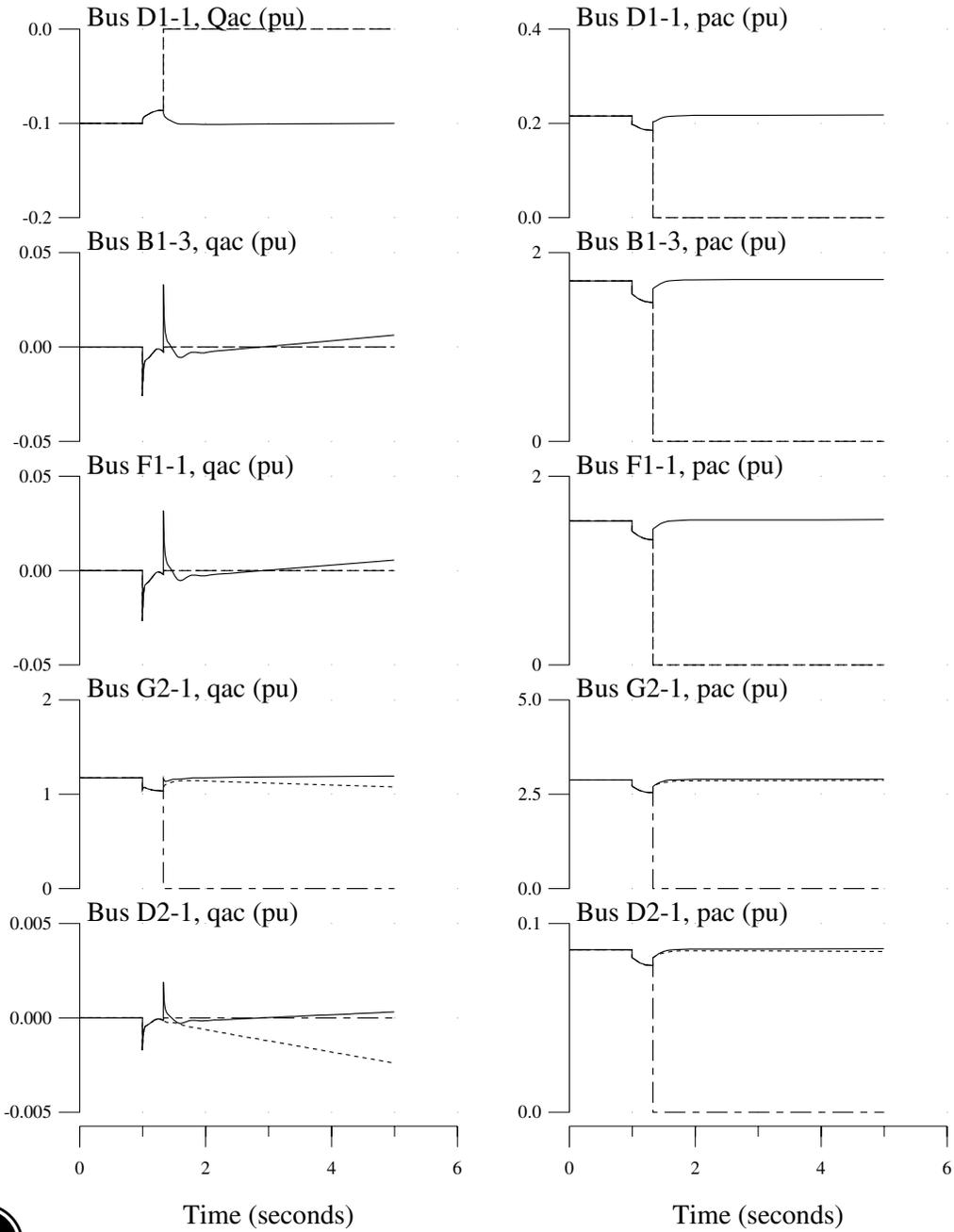
Time (seconds)

19-JUN-2001 15:31:39 out\psfiles\mg2-nodg-NC.chan

Time (seconds)

Page 2

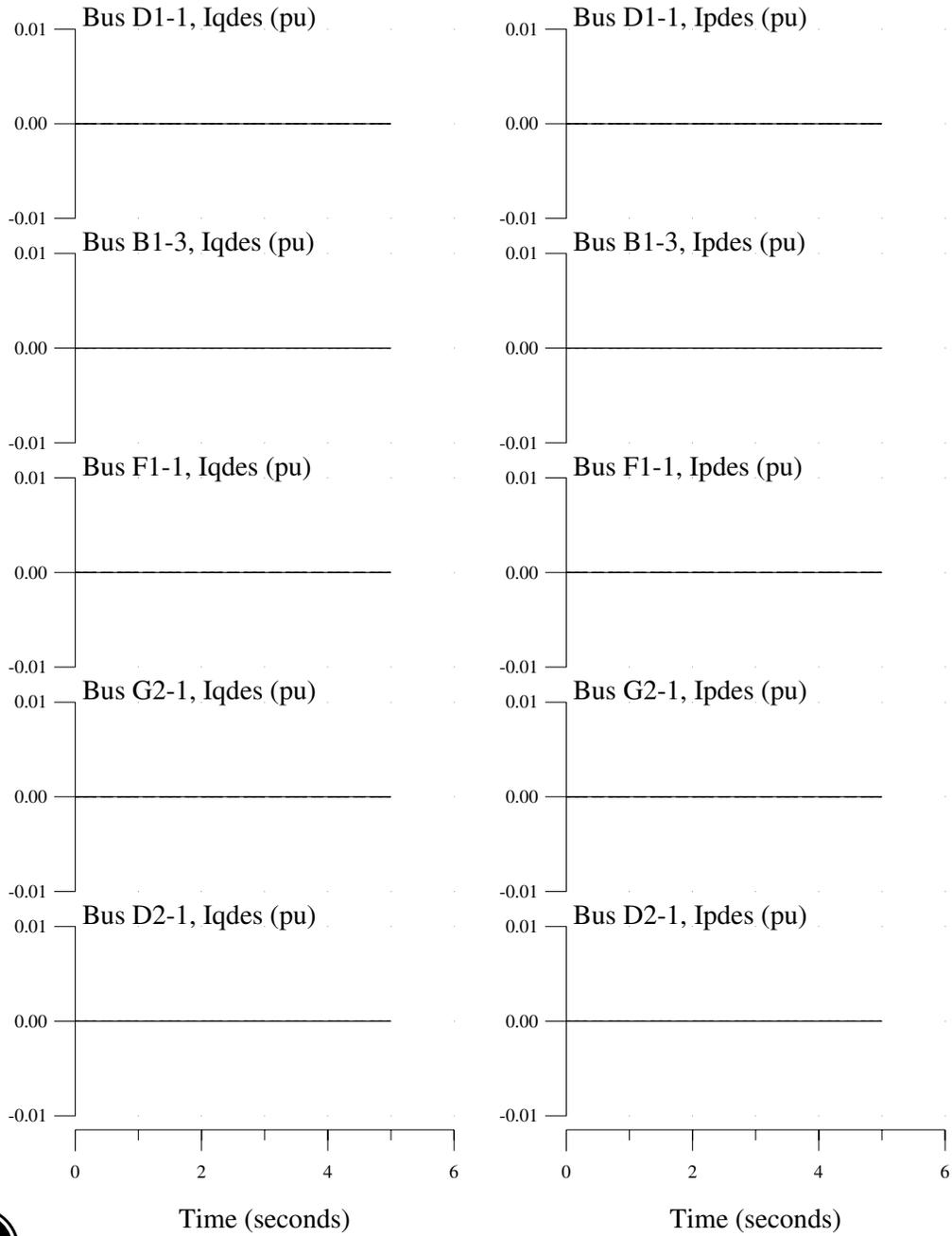
System 2: Without Controls  
 DG Active and Reactive Power  
 no DG trip (\_\_\_\_), 3DG trip ( \_ \_ \_ ), all DG trip ( \_ \_ \_ \_ )



### System 2: Without Controls

#### DG Control Signals

no DG trip (\_\_\_), 3DG trip (\_ \_ \_), all DG trip ( \_ \_ \_ )



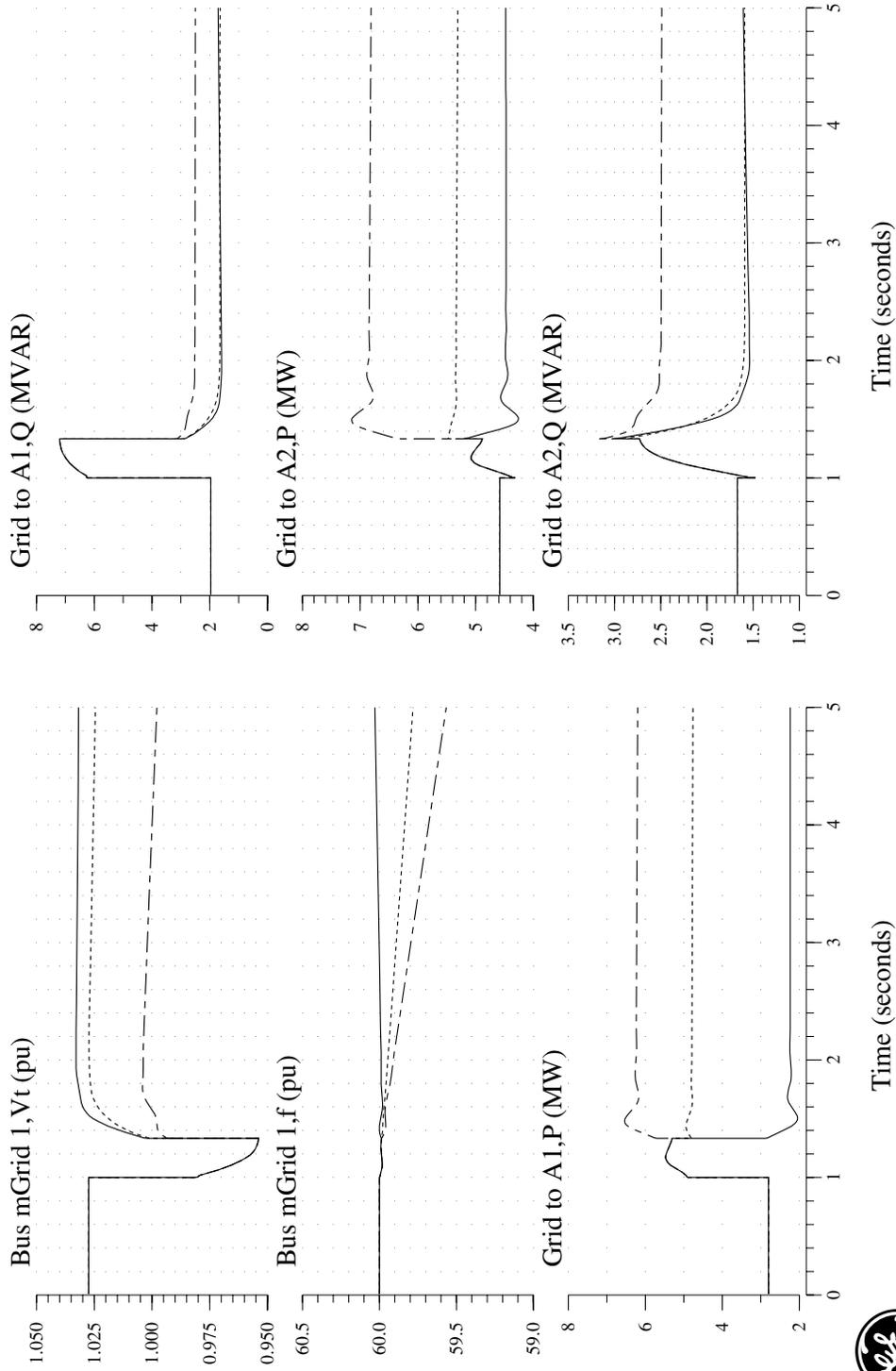
## **SEPARATOR 2: P2 SYSTEM RESPONSE TO A LATERAL FAULT**

All inverter-based DGs with constant power control

# System 2: Power Control

## System Quantities

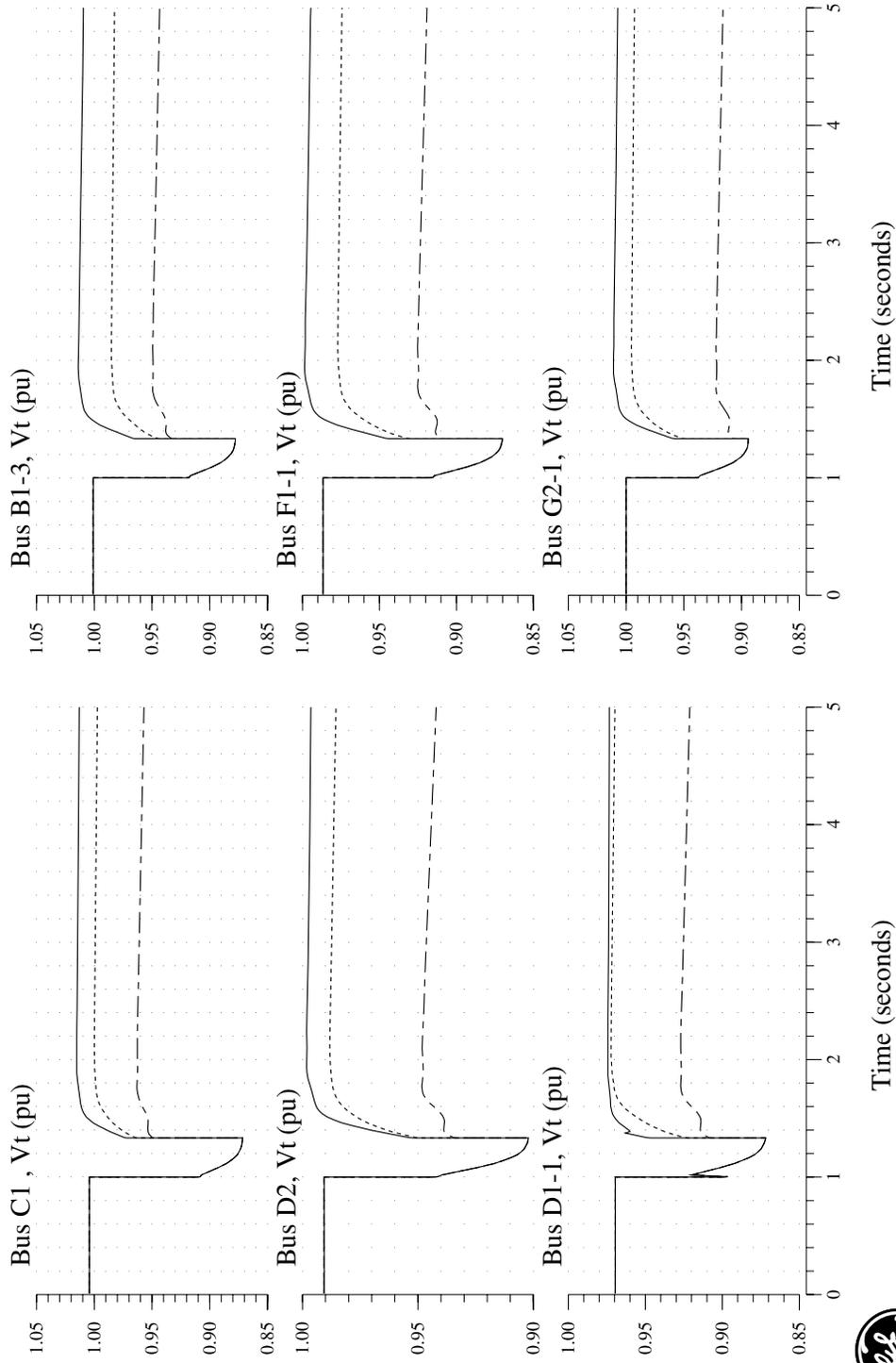
no DG trip (—), 3DG trip (---), all DG trip (----



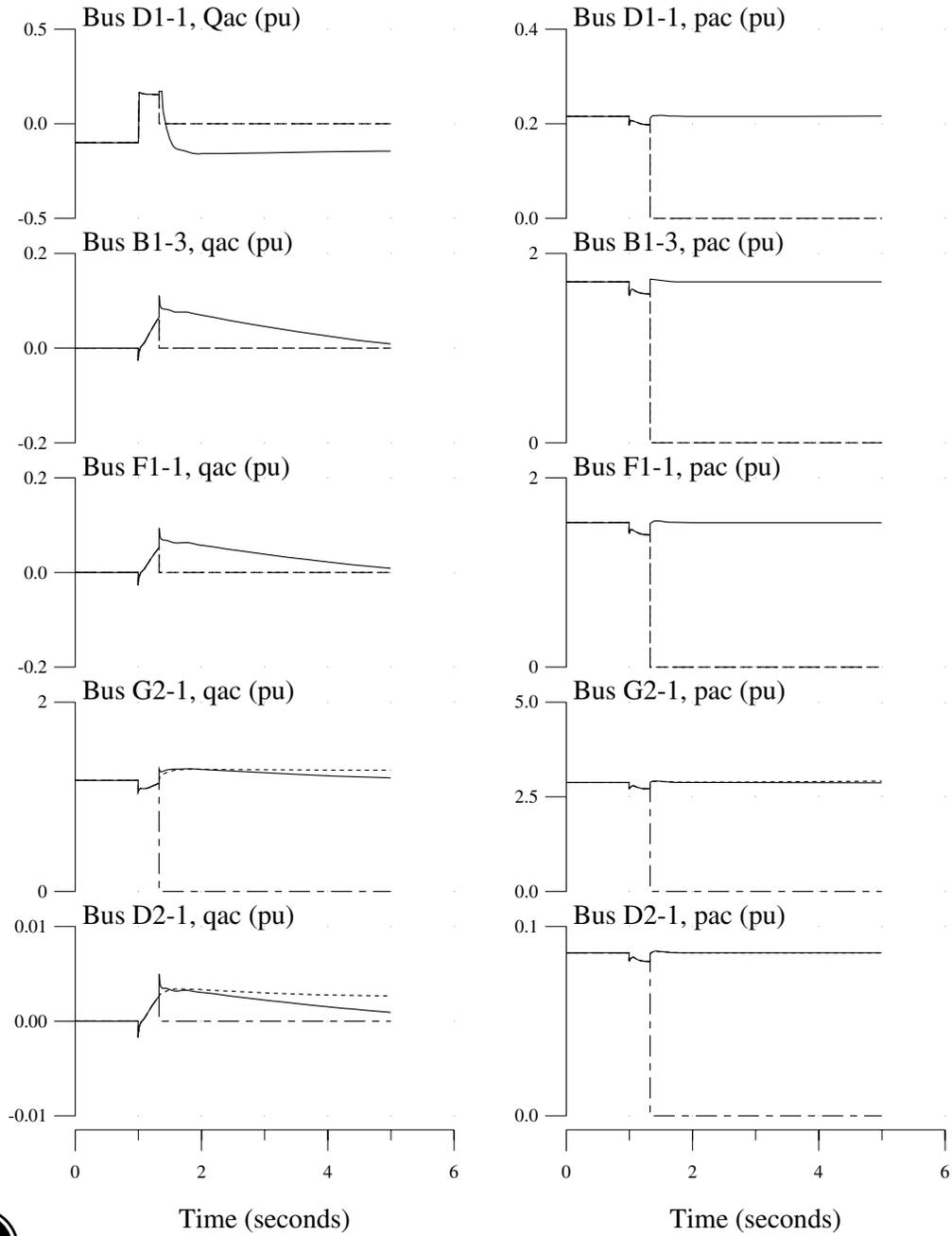
# System 2: Power Control

## Voltages

no DG trip (—), 3DG trip (---), all DG trip (---)



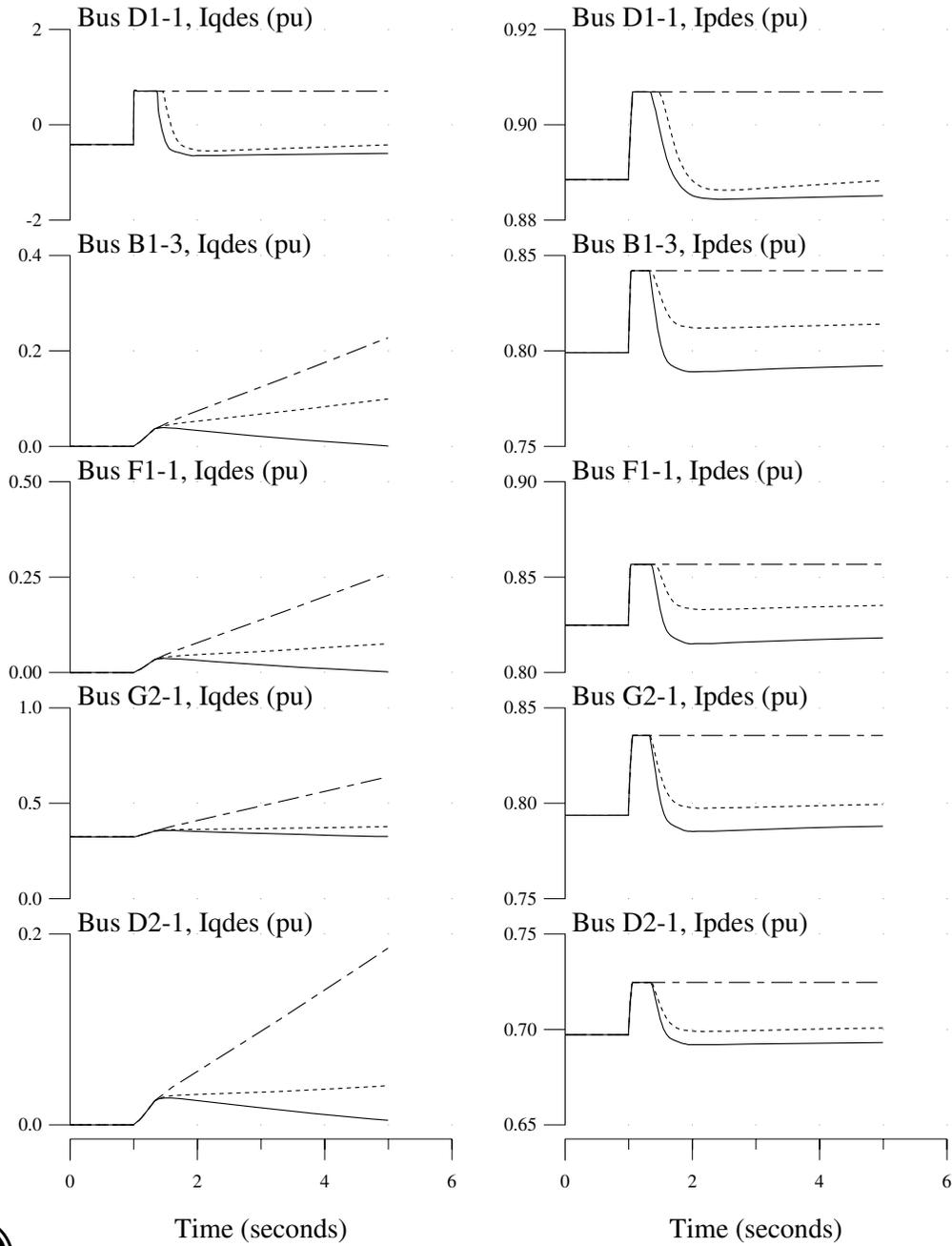
System 2: Power Control  
 DG Active and Reactive Power  
 no DG trip (\_\_\_\_), 3DG trip ( \_ \_ \_ ), all DG trip ( \_ \_ \_ \_ )



## System 2: Power Control

### DG Control Signals

no DG trip (\_\_\_\_), 3DG trip (\_ \_ \_), all DG trip ( \_ \_ \_ )



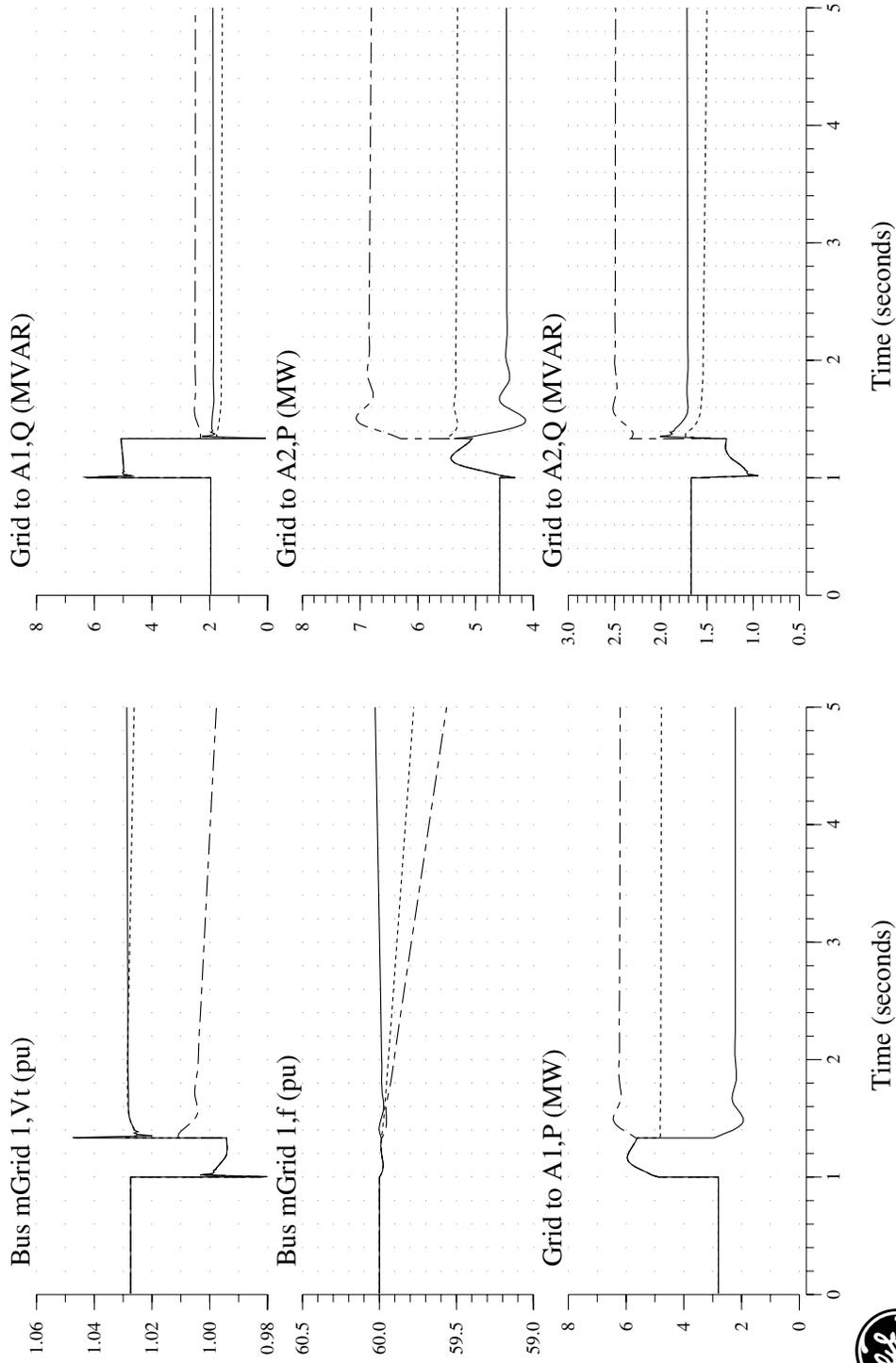
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**SEPARATOR 3: P2 SYSTEM RESPONSE TO A LATERAL FAULT**  
All inverter-based DGs with high gain voltage control

## System 2: Voltage Control

### System Quantities

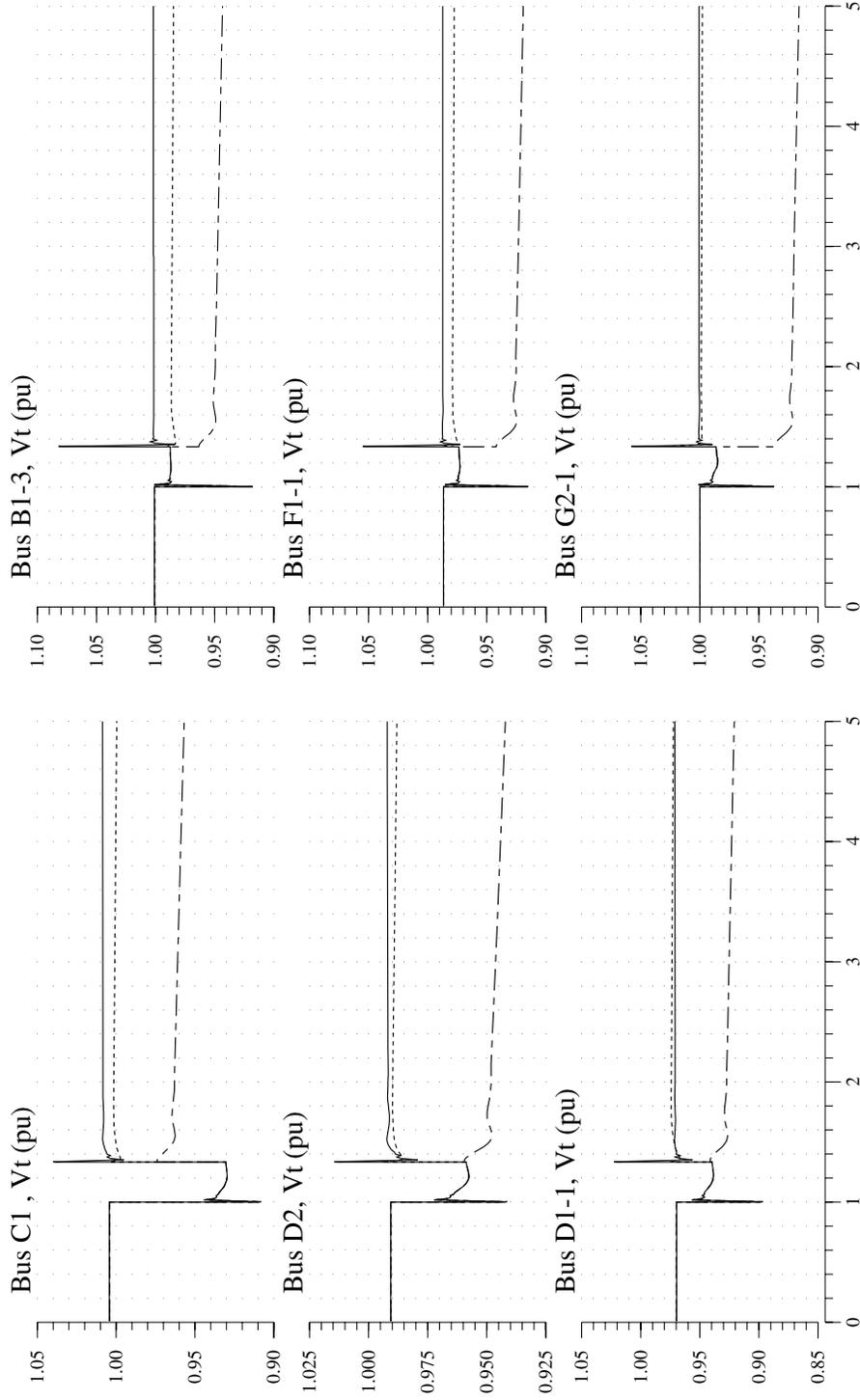
no DG trip (—), 3DG trip (---), all DG trip (----)



# System 2: Voltage Control

## Voltages

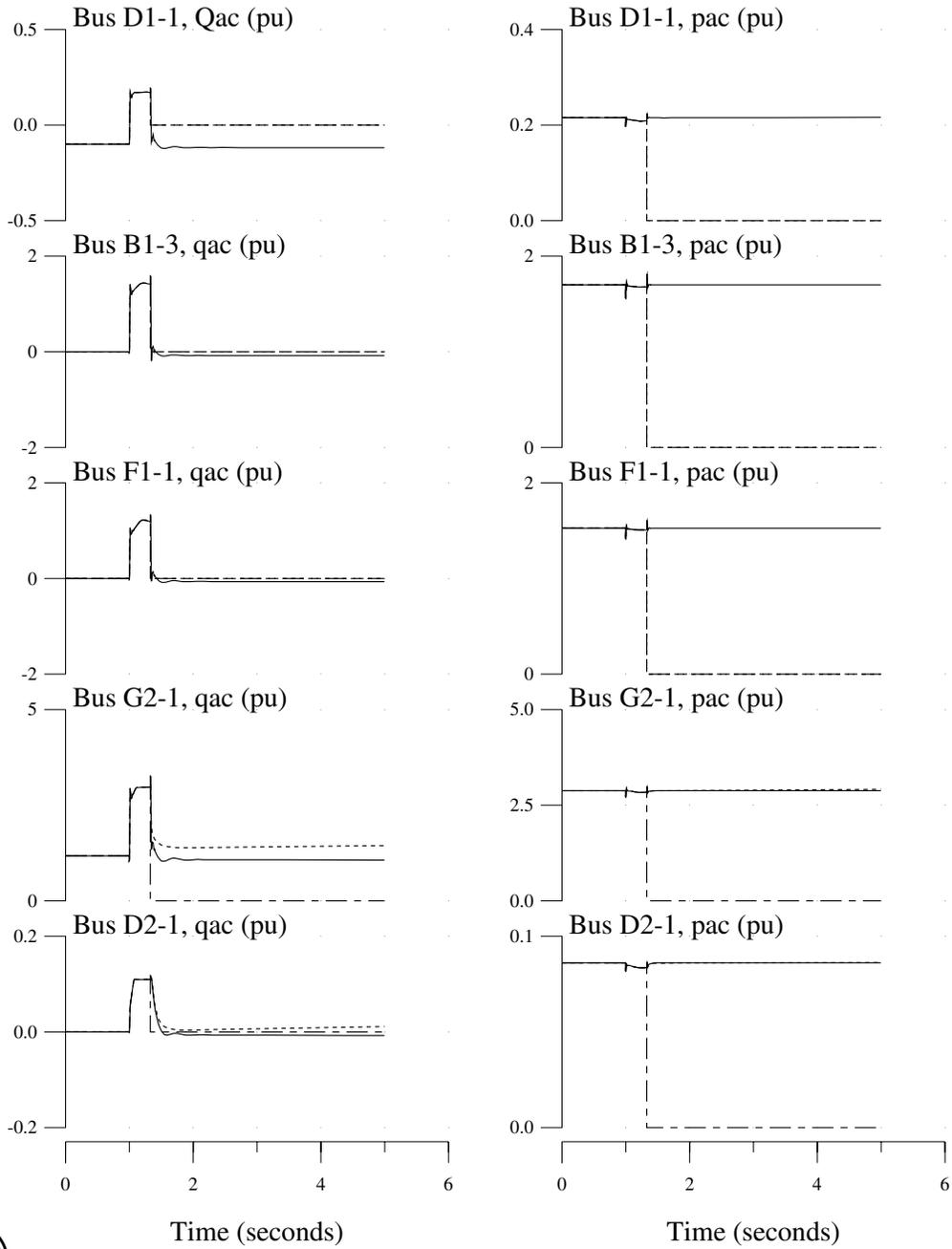
no DG trip (—), 3DG trip (---), all DG trip (---)



Time (seconds)

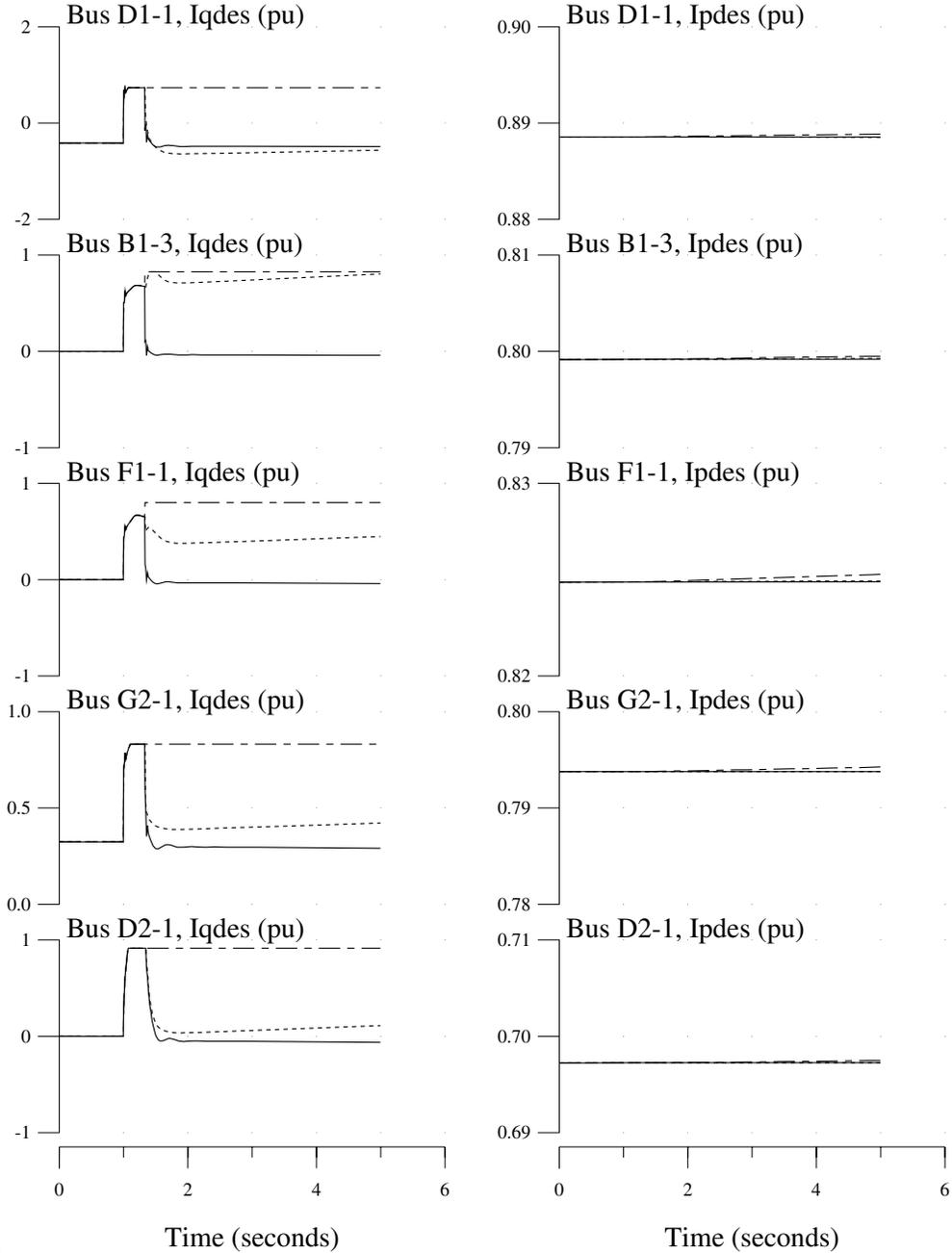
Time (seconds)

System 2: Voltage Control  
 DG Active and Reactive Power  
 no DG trip (\_\_\_\_), 3DG trip ( \_ \_ \_ ), all DG trip ( \_ \_ \_ \_ )



## System 2: Voltage Control DG Control Signals

no DG trip (\_\_\_), 3DG trip (\_\_\_), all DG trip (\_\_\_)



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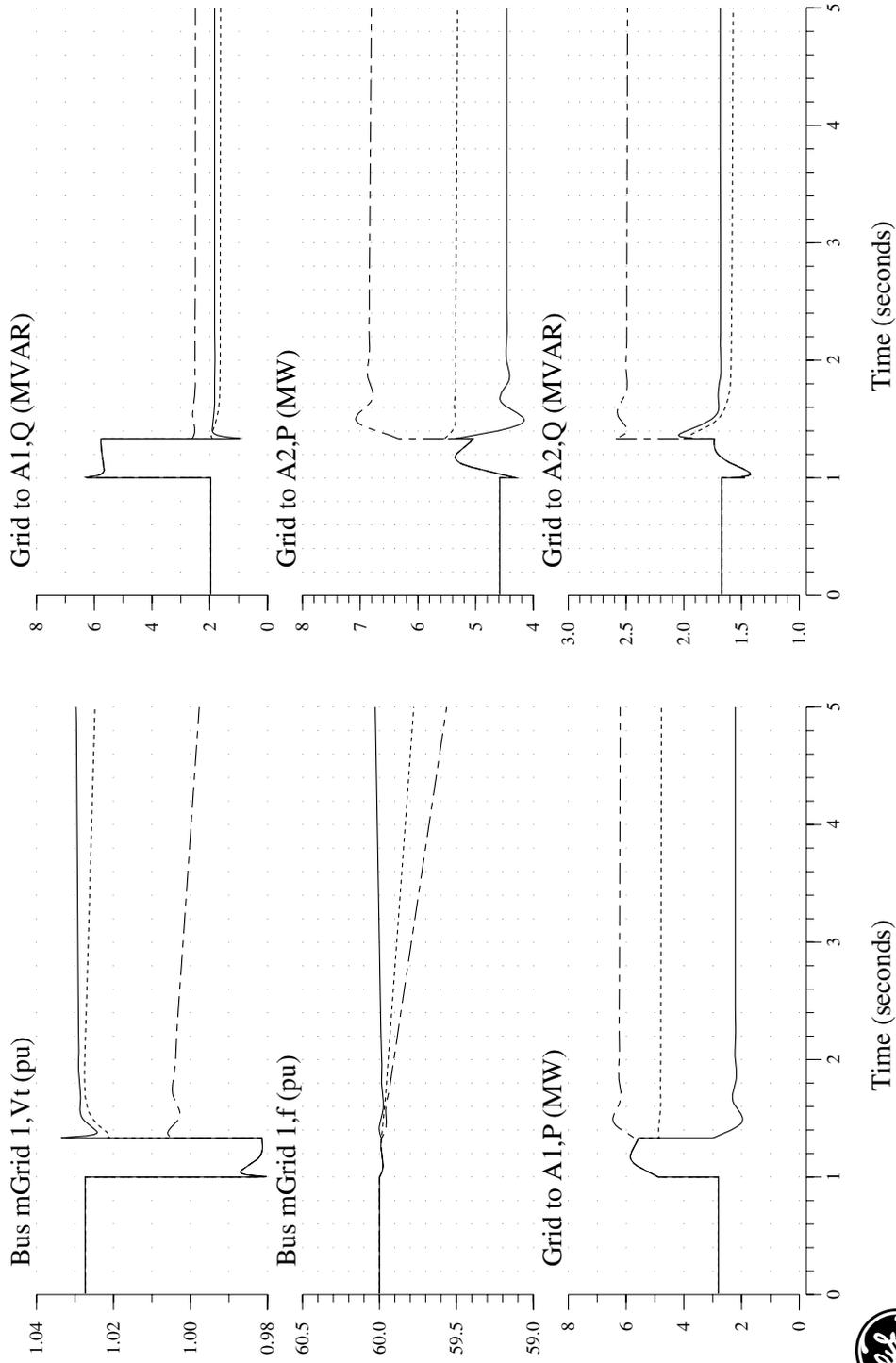
**SEPARATOR 4: P2 SYSTEM RESPONSE TO A LATERAL FAULT**

All inverter-based DGs with moderate gain voltage control

## System 2: Voltage Control

### System Quantities

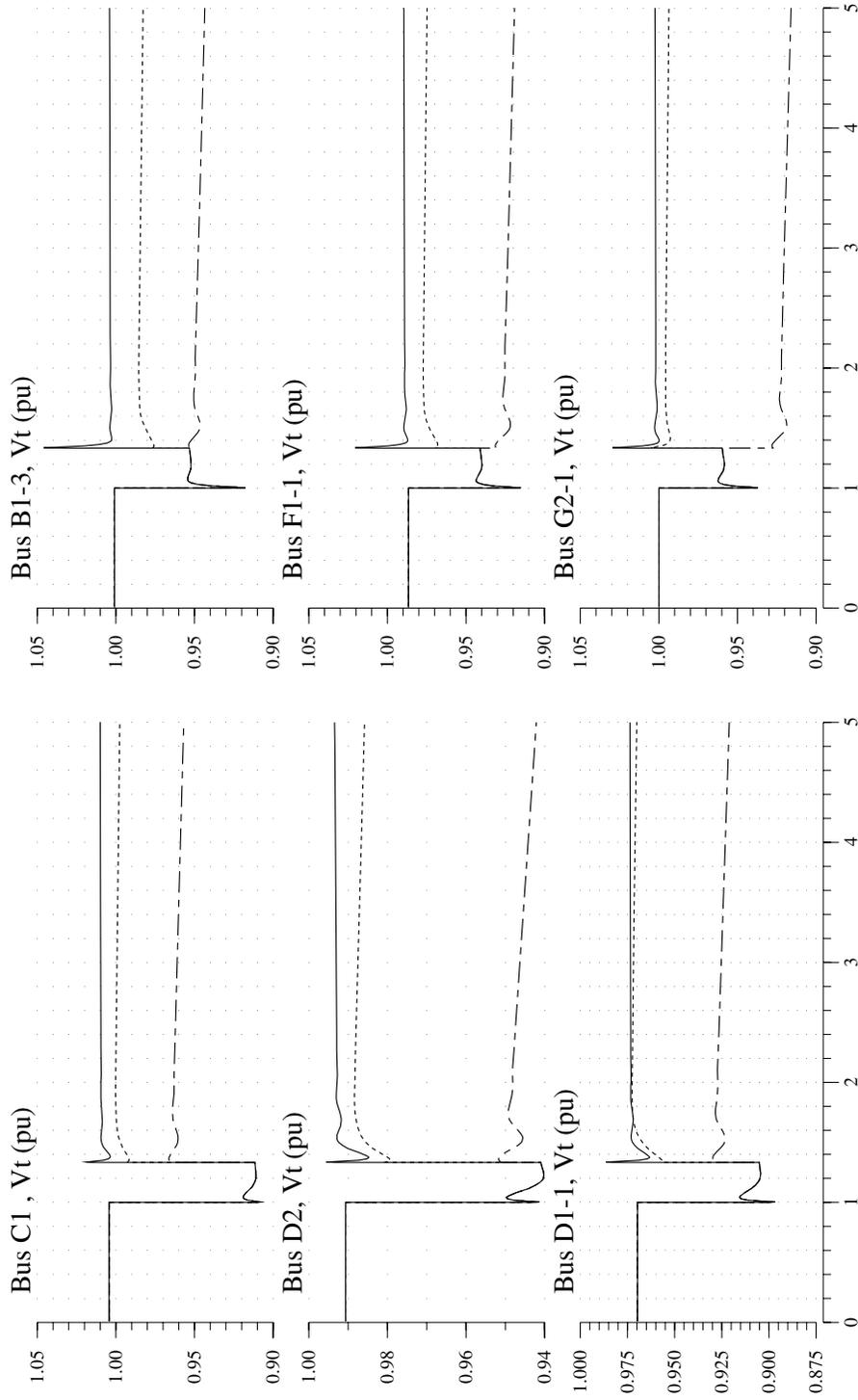
no DG trip (—), 3DG trip (---), all DG trip (----)



# System 2: Voltage Control

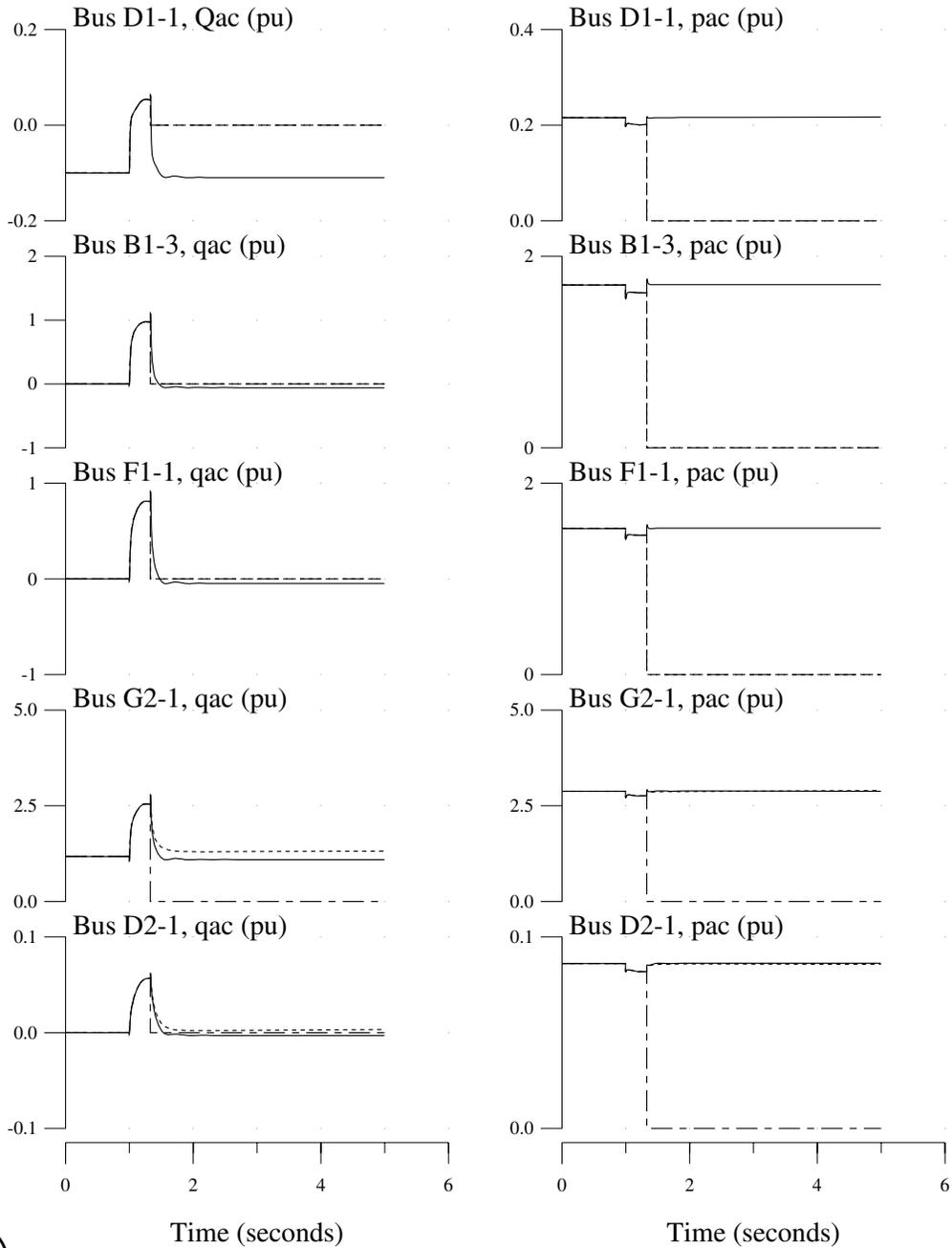
## Voltages

no DG trip (—), 3DG trip (---), all DG trip (---)



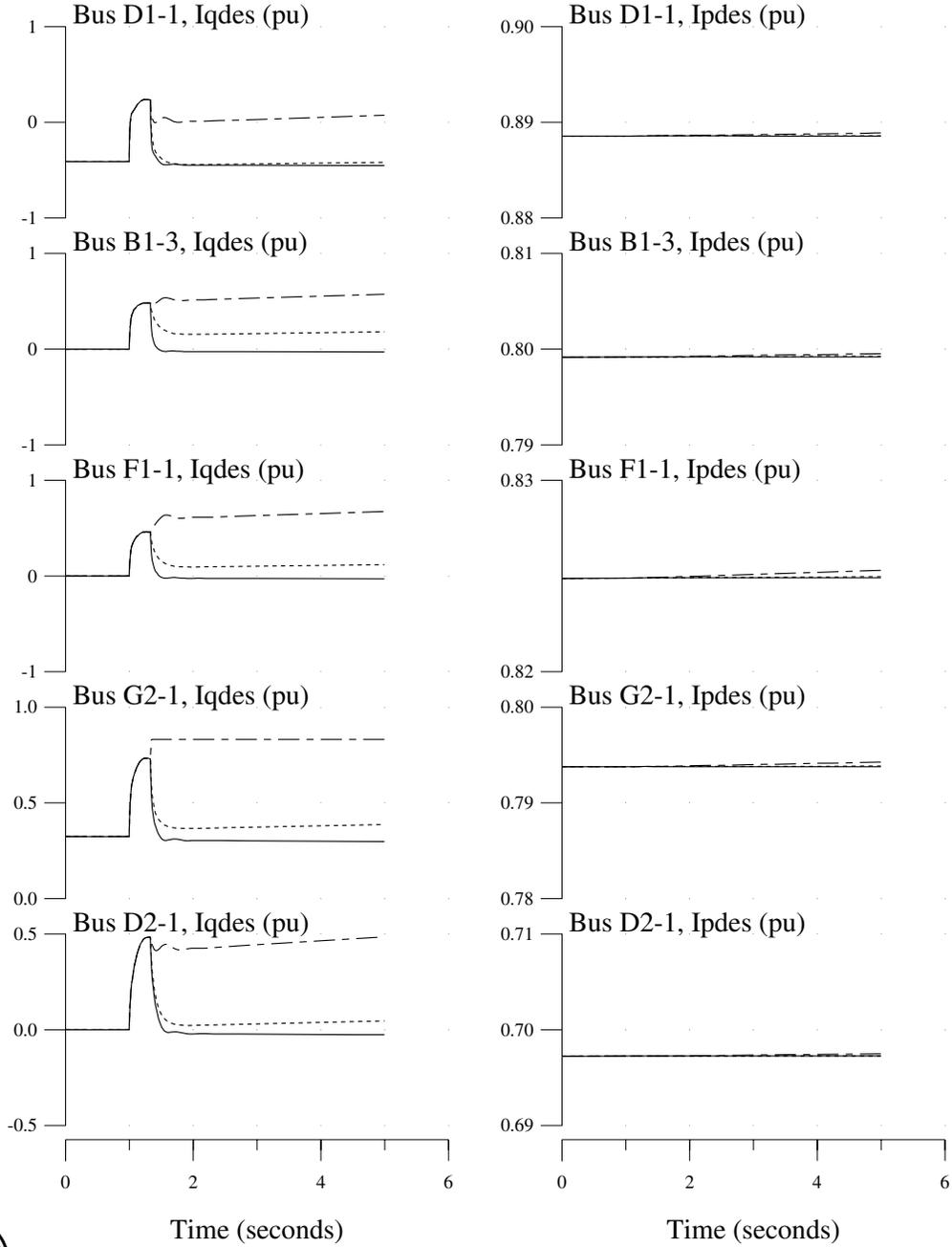
Time (seconds)

System 2: Voltage Control  
 DG Active and Reactive Power  
 no DG trip (\_\_\_\_), 3DG trip ( \_ \_ \_ ), all DG trip ( \_ \_ \_ \_ )



## System 2: Voltage Control DG Control Signals

no DG trip (\_\_\_\_), 3DG trip (\_ \_ \_), all DG trip ( \_ \_ \_ )



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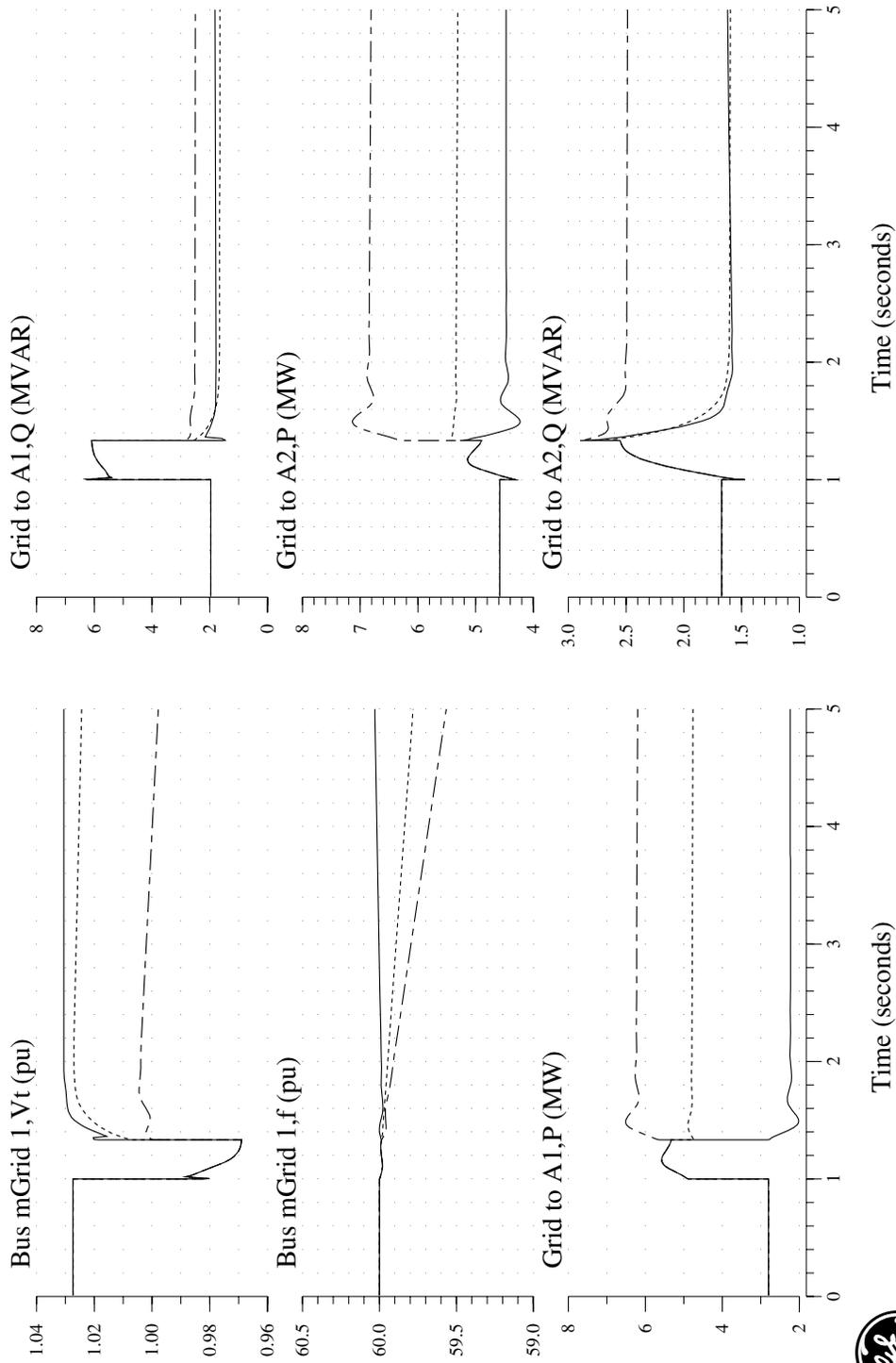
**SEPARATOR 5: P2 SYSTEM RESPONSE TO A LATERAL FAULT**

All inverter-based DGs with high gain voltage control and constant power control

# System 2: Power and Voltage Control

## System Quantities

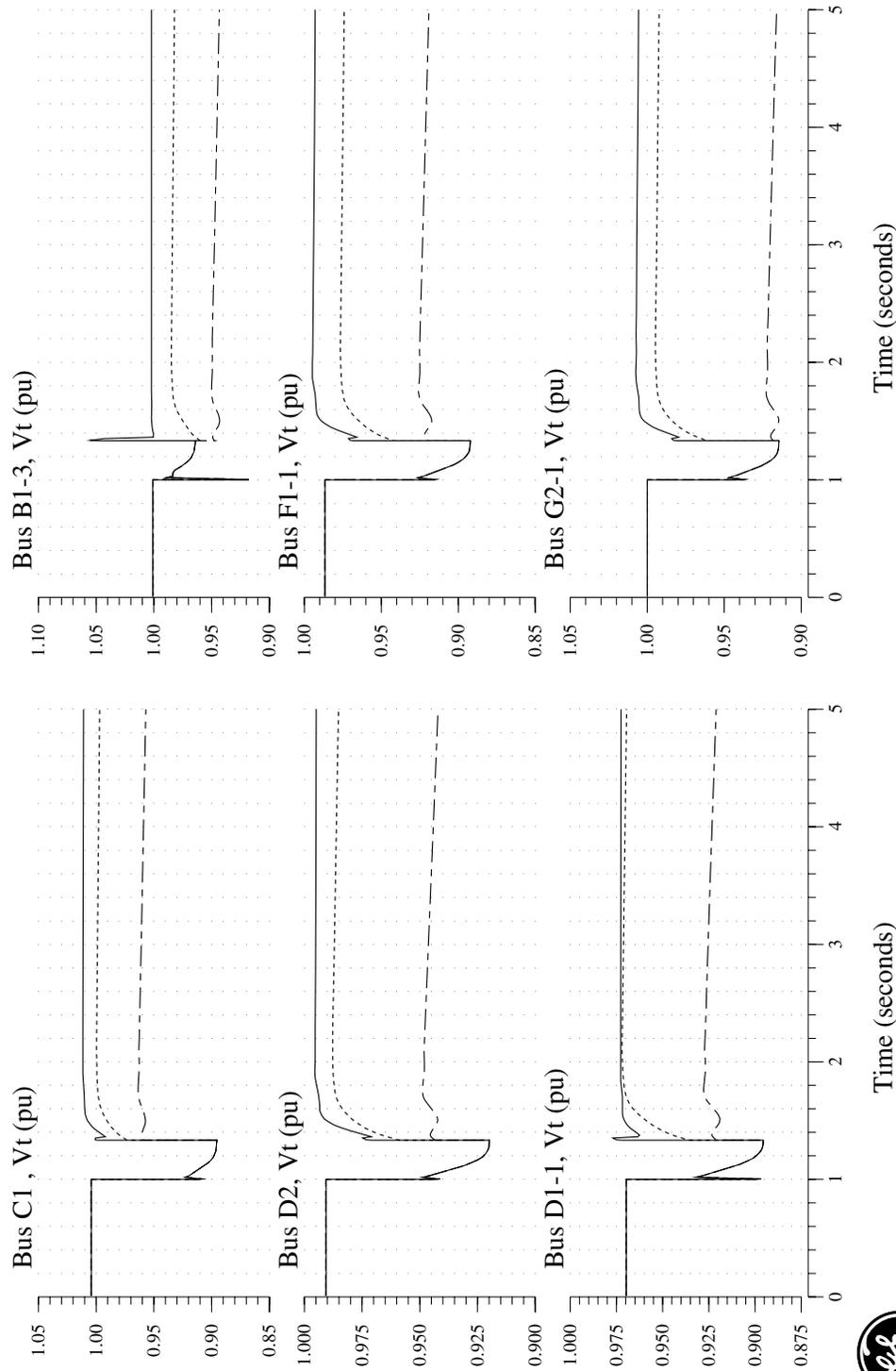
no DG trip (—), 3DG trip (---), all DG trip (----



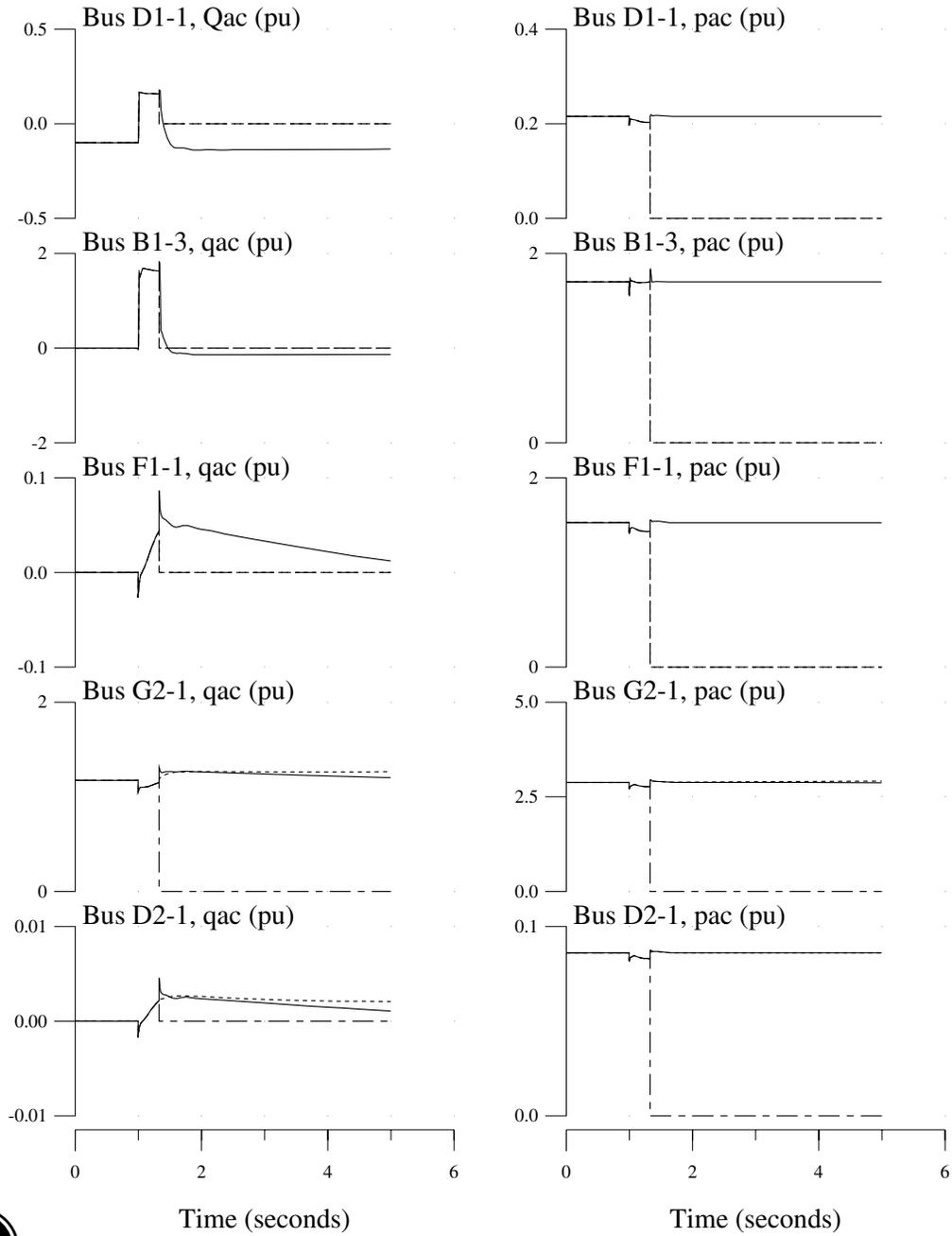
# System 2: Power and Voltage Control

## Voltages

no DG trip (—), 3DG trip (---), all DG trip (---)

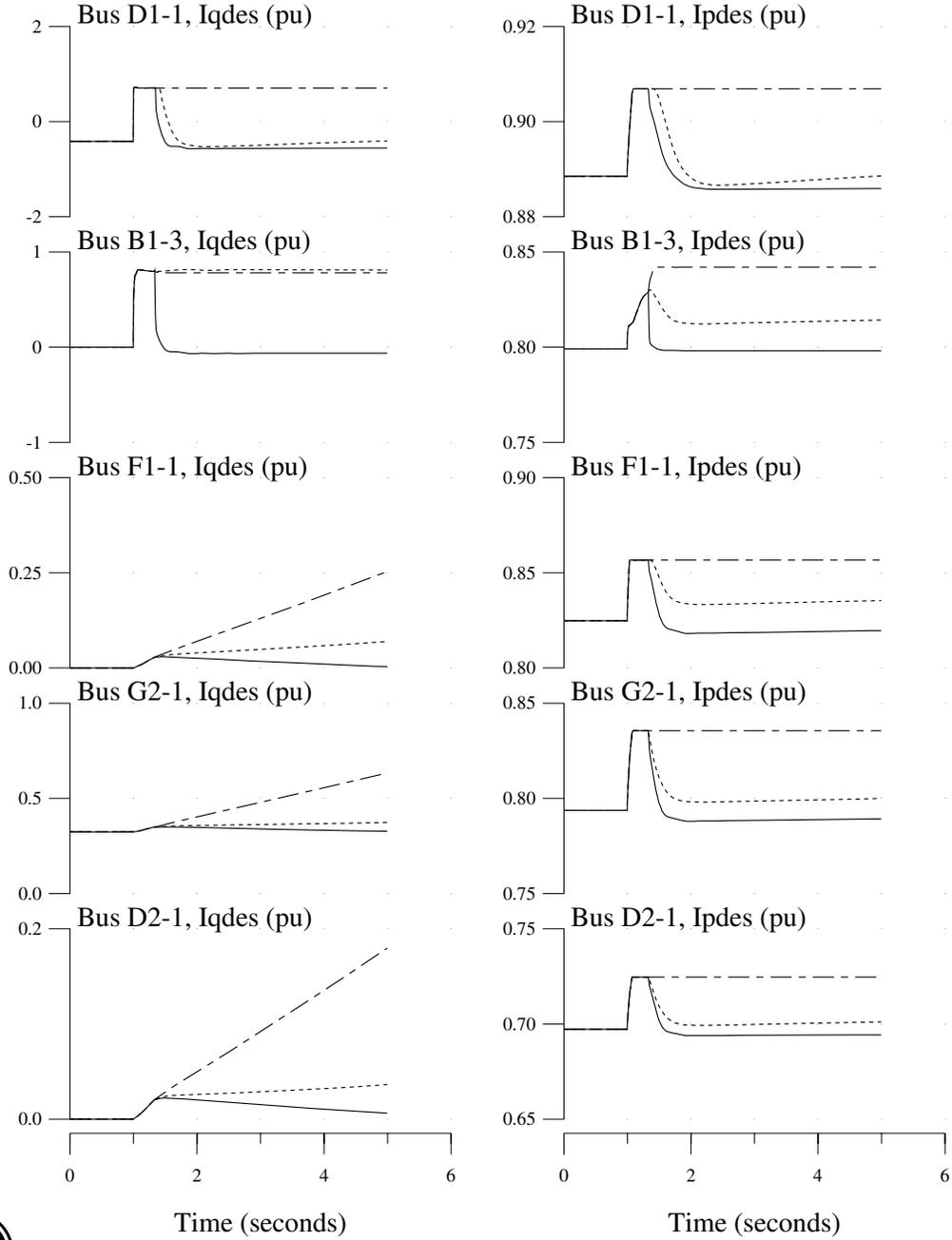


System 2: Power and Voltage Control  
 DG Active and Reactive Power  
 no DG trip (\_\_\_\_), 3DG trip (\_ \_ \_), all DG trip ( \_ \_ \_ )



## System 2: Power and Voltage Control DG Control Signals

no DG trip (\_\_\_), 3DG trip (\_\_\_), all DG trip (\_\_\_)



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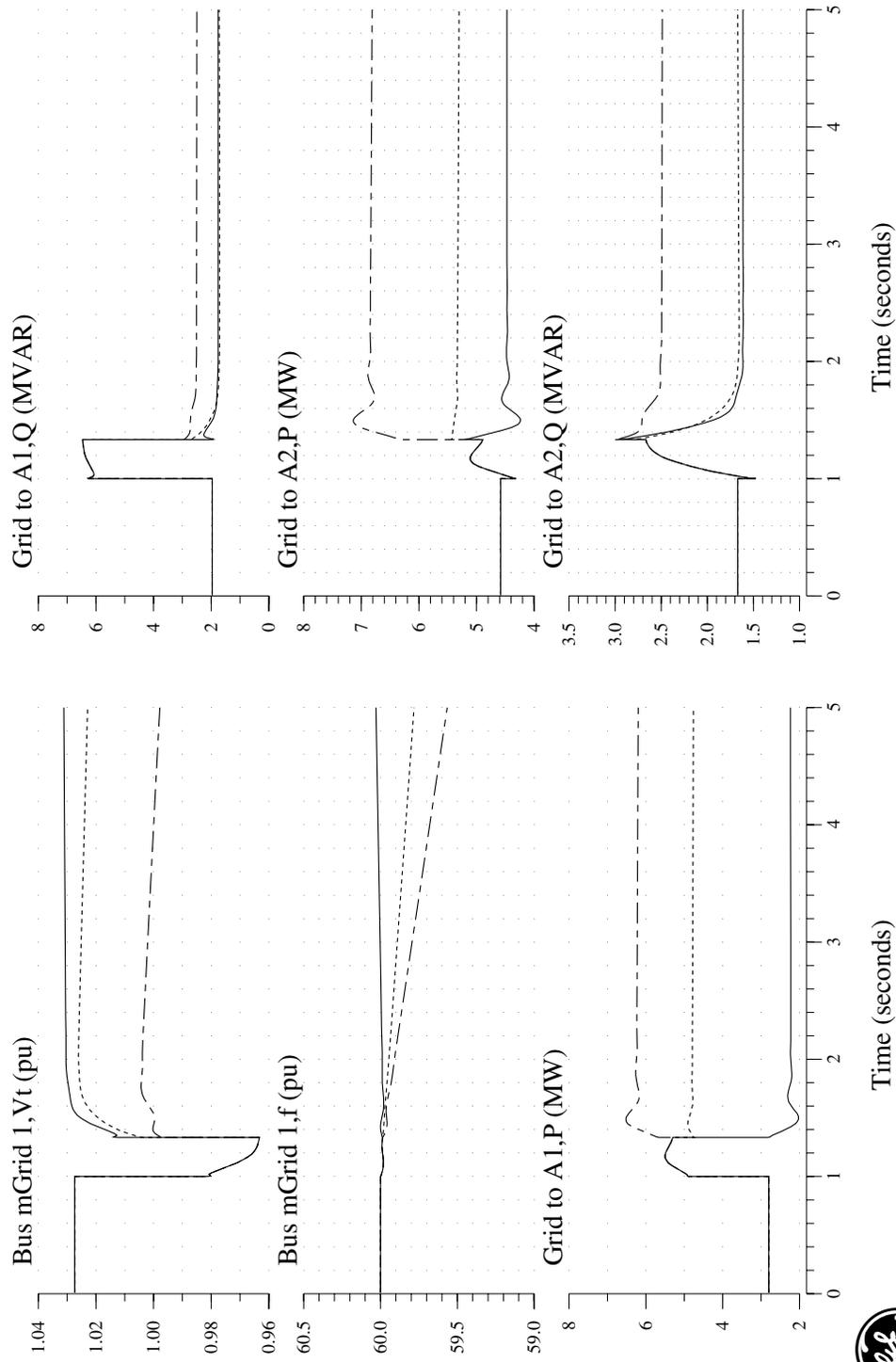
**SEPARATOR 6: P2 SYSTEM RESPONSE TO A LATERAL FAULT**

All inverter-based DGs with moderate gain voltage control and constant power control

## System 2: Power and Voltage Control

### System Quantities

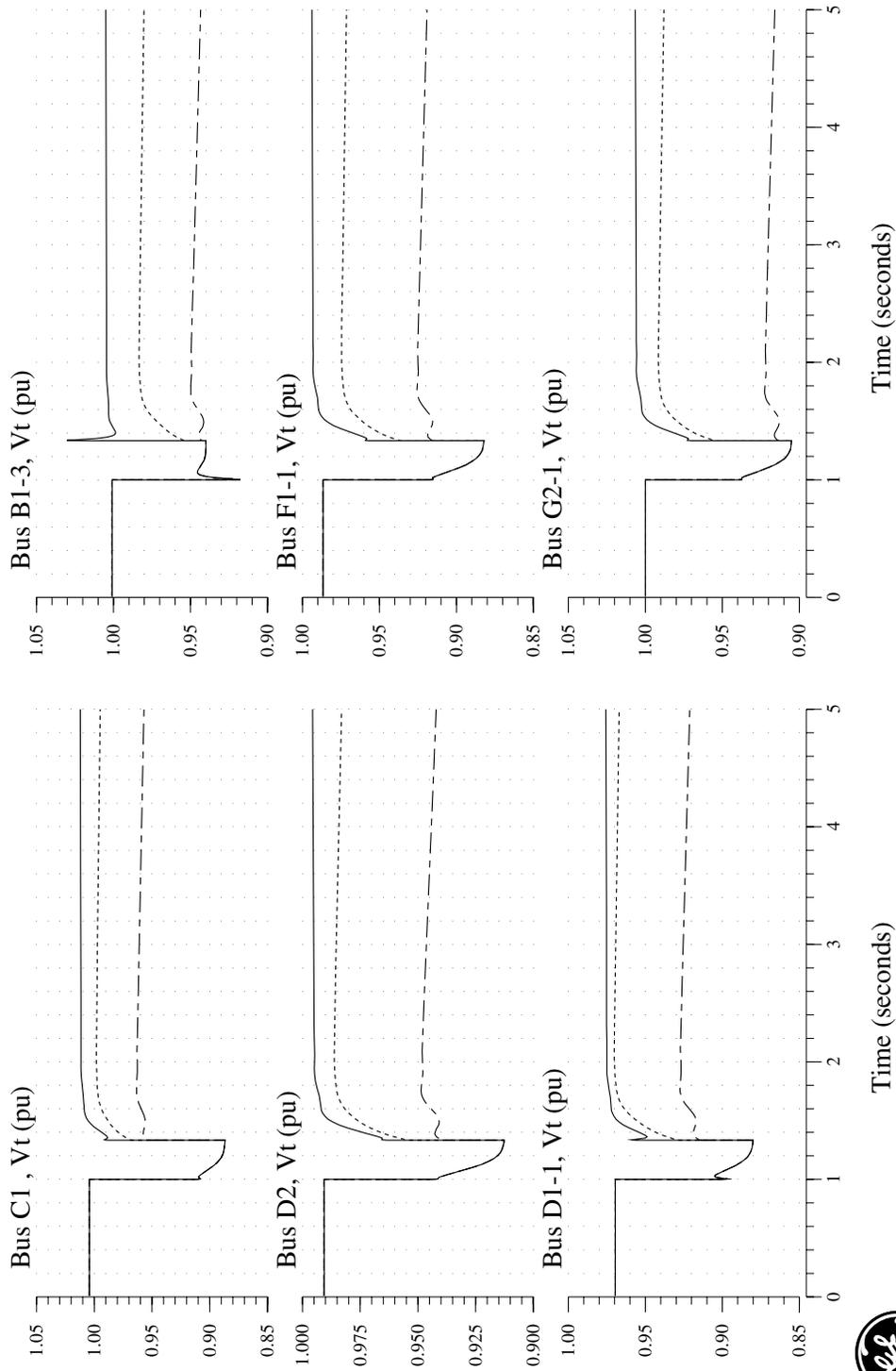
no DG trip (—), 3DG trip (---), all DG trip (----



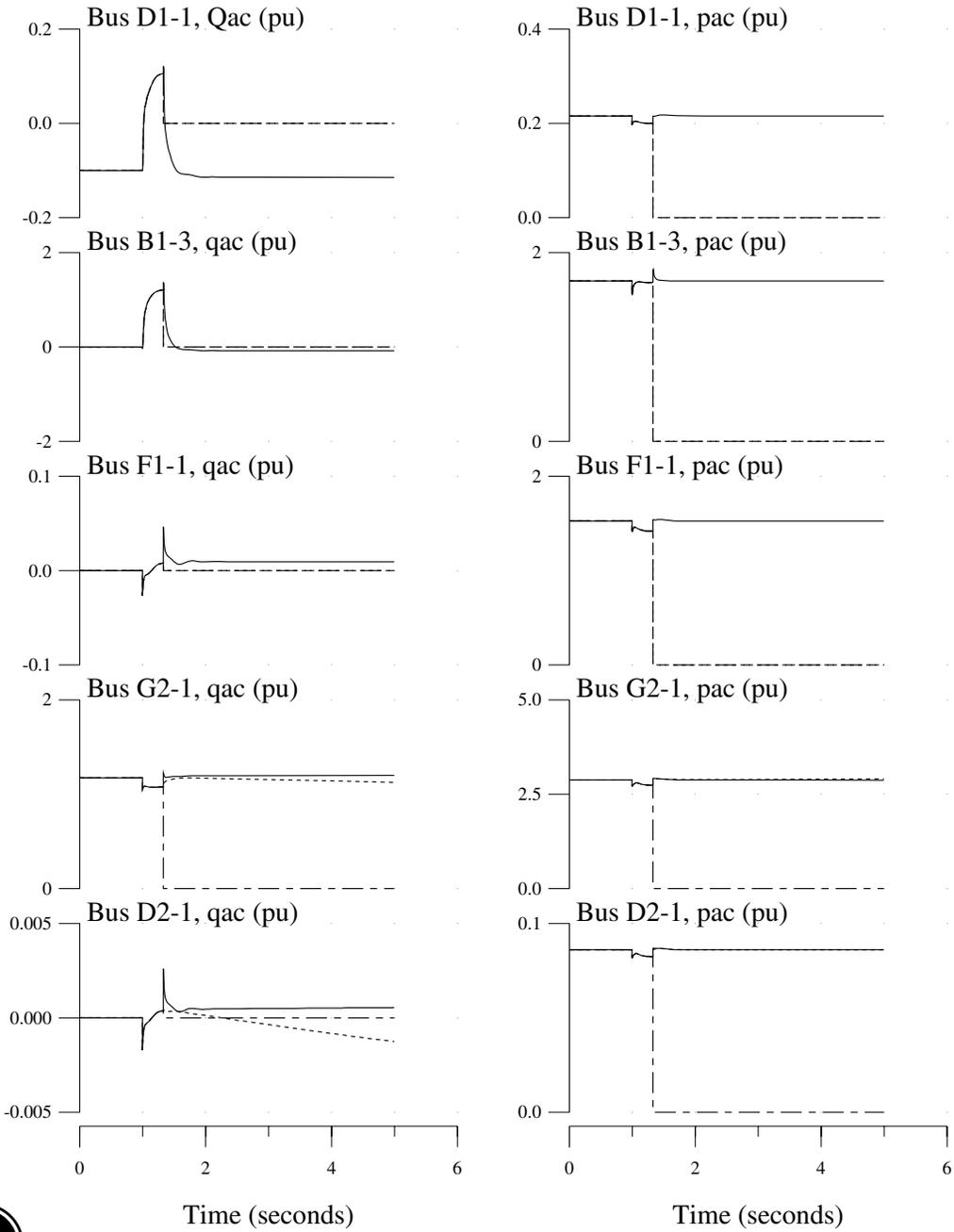
# System 2: Power and Voltage Control

## Voltages

no DG trip (—), 3DG trip (---), all DG trip (---)

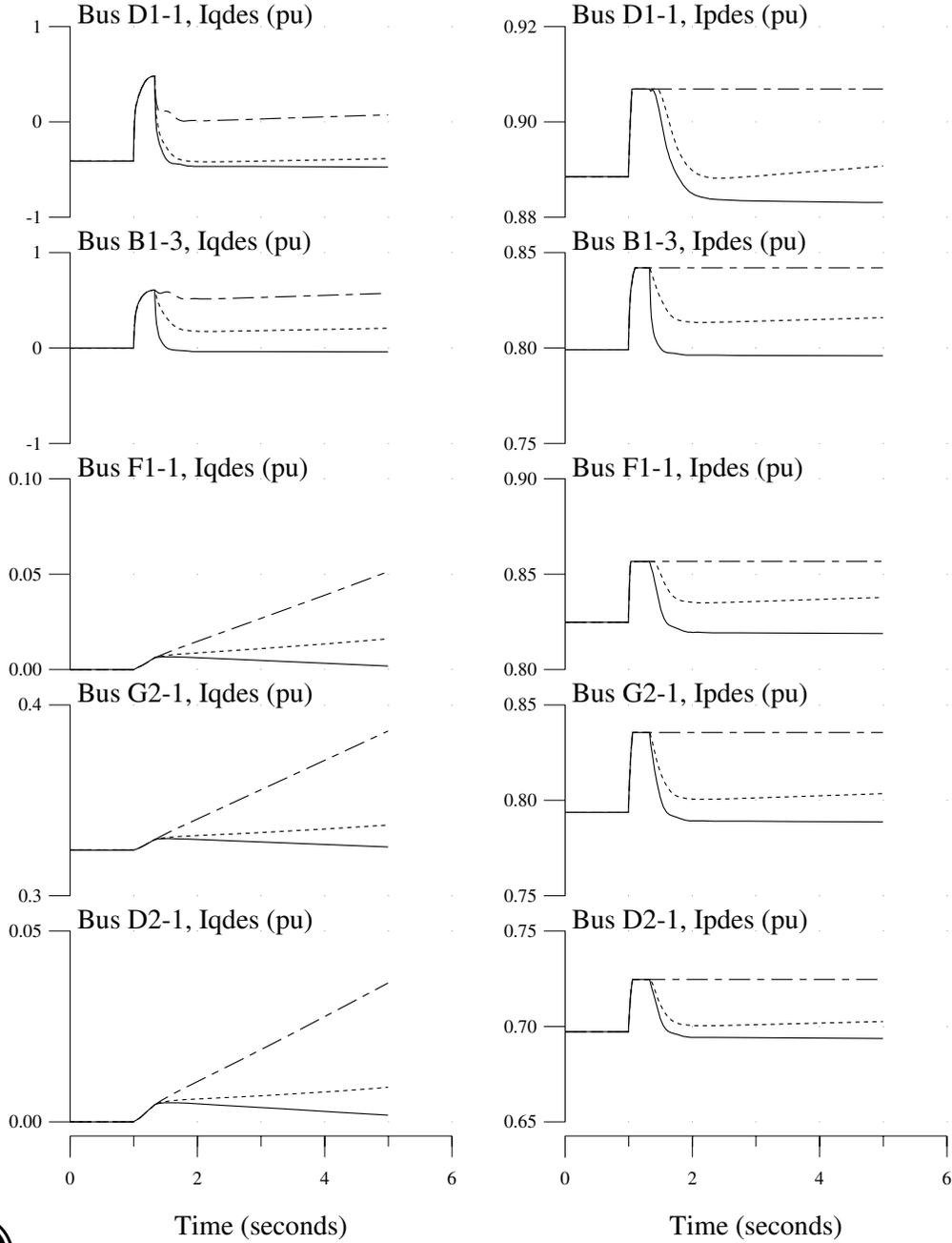


System 2: Power and Voltage Control  
 DG Active and Reactive Power  
 no DG trip (\_\_\_\_), 3DG trip (\_ \_ \_), all DG trip ( \_ \_ \_ )



## System 2: Power and Voltage Control DG Control Signals

no DG trip (\_\_\_\_), 3DG trip ( \_ \_ \_ ), all DG trip ( \_ \_ \_ \_ )



# Appendix G. Microgrid

## **SEPARATOR 1: P2 SYSTEM CONFIGURED AS A MICRO GRID**

All Inverter Based DGs with Voltage and Frequency Regulation  
Response to Trip of Microgrid from the Utility Grid

3 Cases on Each Set of Axes reflect different initial power exchanges with the utility grid:

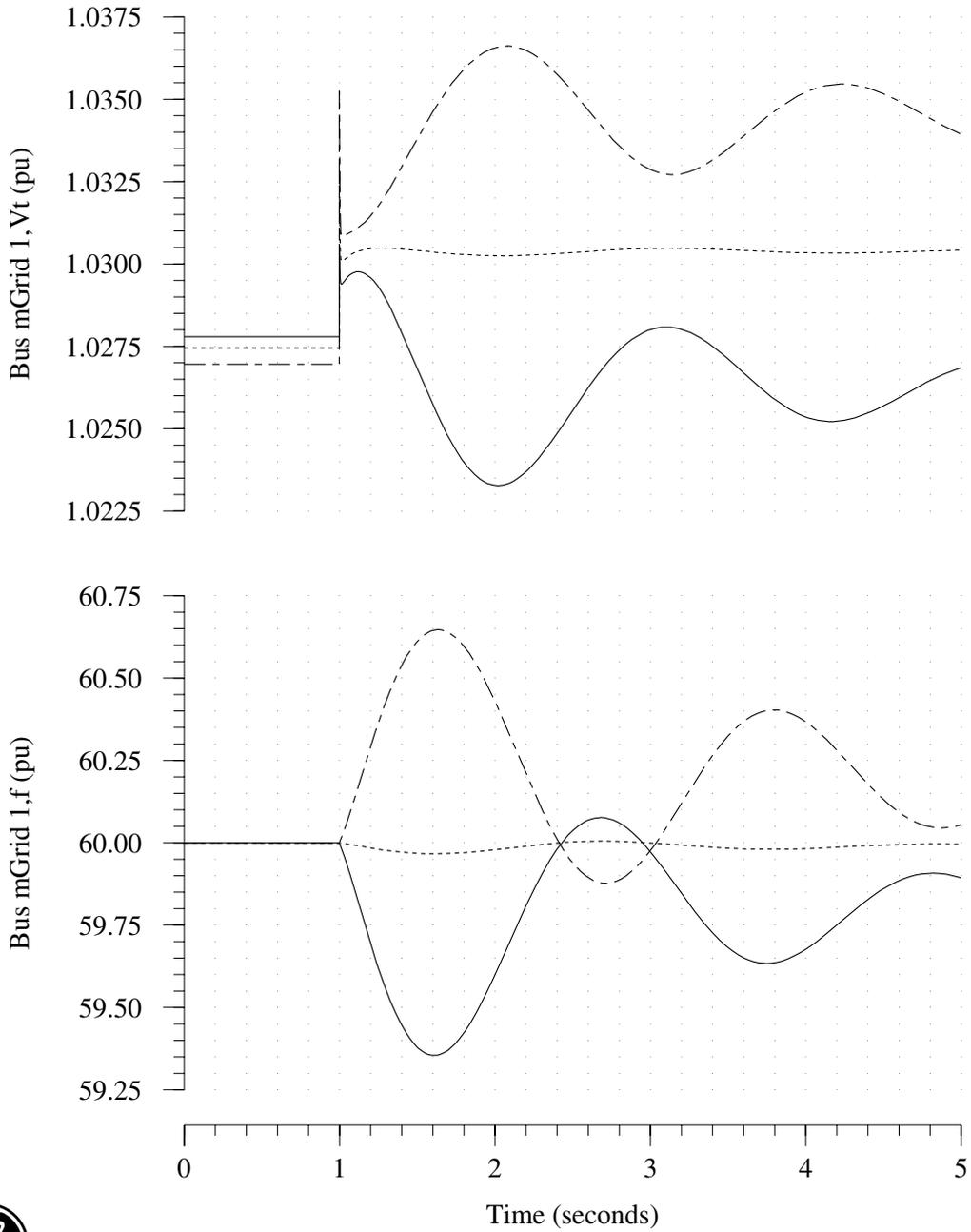
Solid Trace: Microgrid Initially Importing approximately 1 MW.

Dotted Trace: Microgrid Initially nearly balanced (very small import)

Dot-Dash Trace: Microgrid Initially Exporting approximately 1 MW

### System 2: Frequency Regulation System Quantities

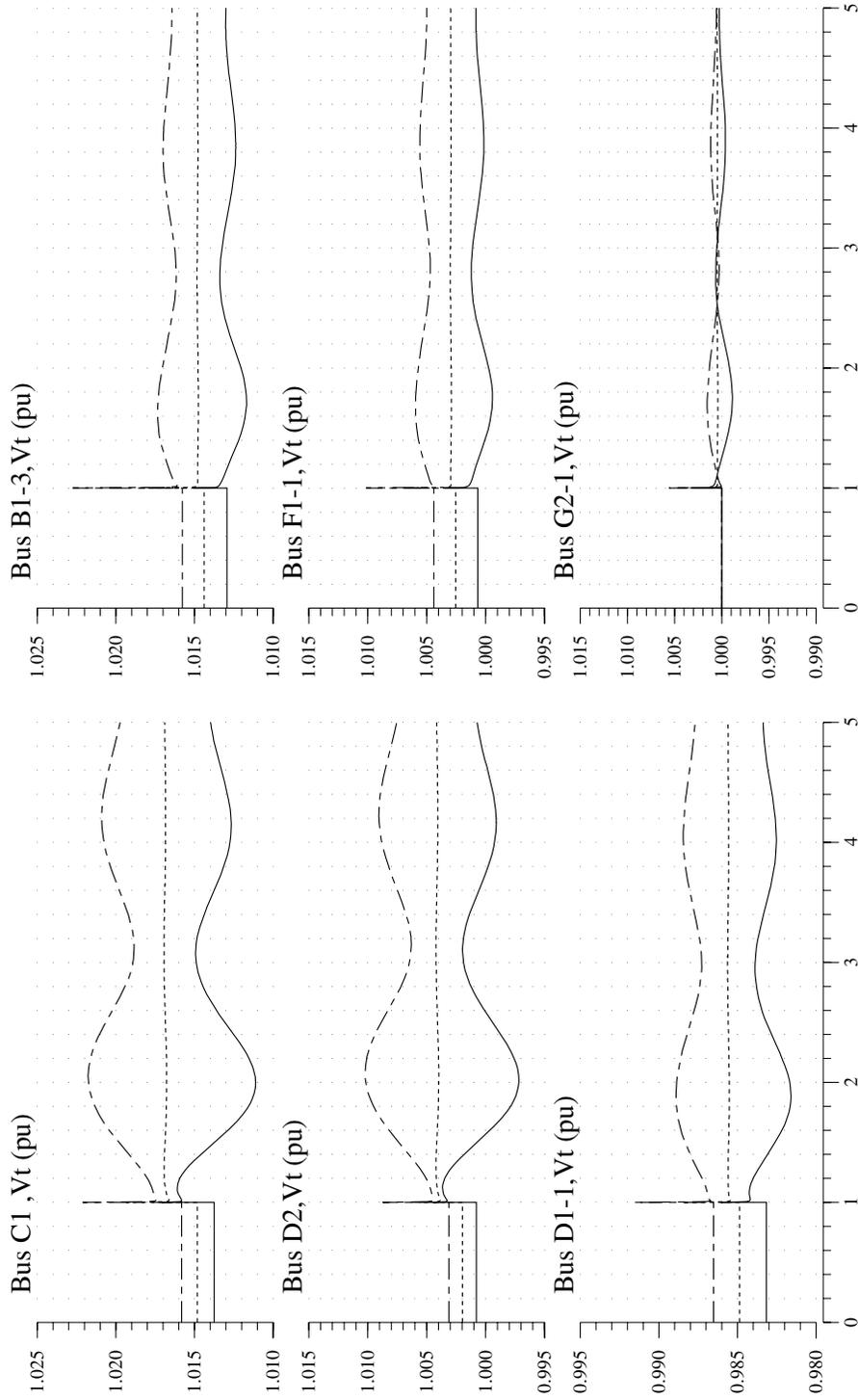
Initial power from the external grid +2MW(\_\_\_\_),+1MW(- -),+0MW(\_\_\_\_),-1MW(\_\_\_\_),isl(\_\_\_\_)



# System 2: Frequency Regulation

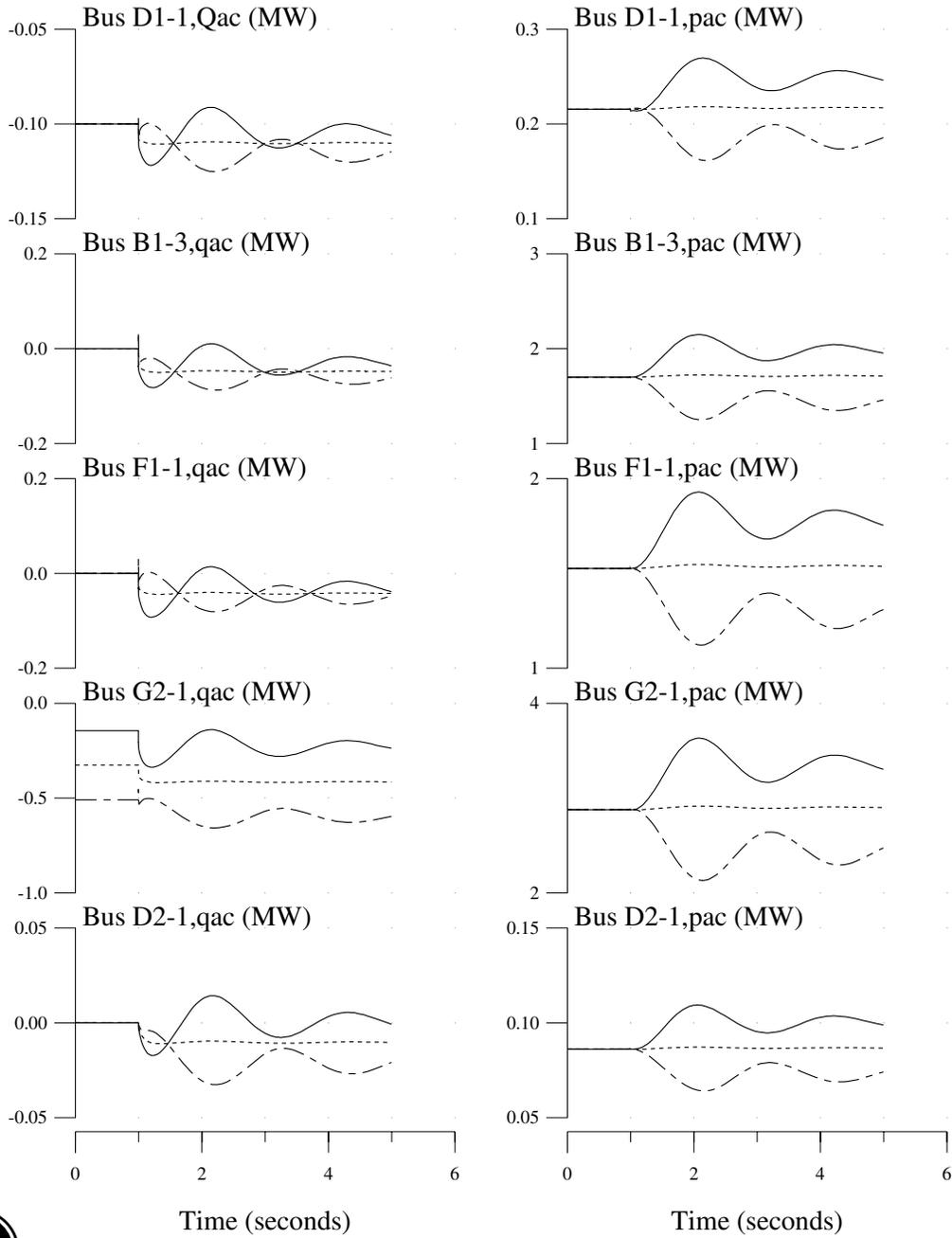
## Voltages

Initial power from the external grid +2MW(\_\_\_\_),+1MW(- -),+0MW(\_\_\_\_),-1MW(\_\_\_\_),isl(- -)



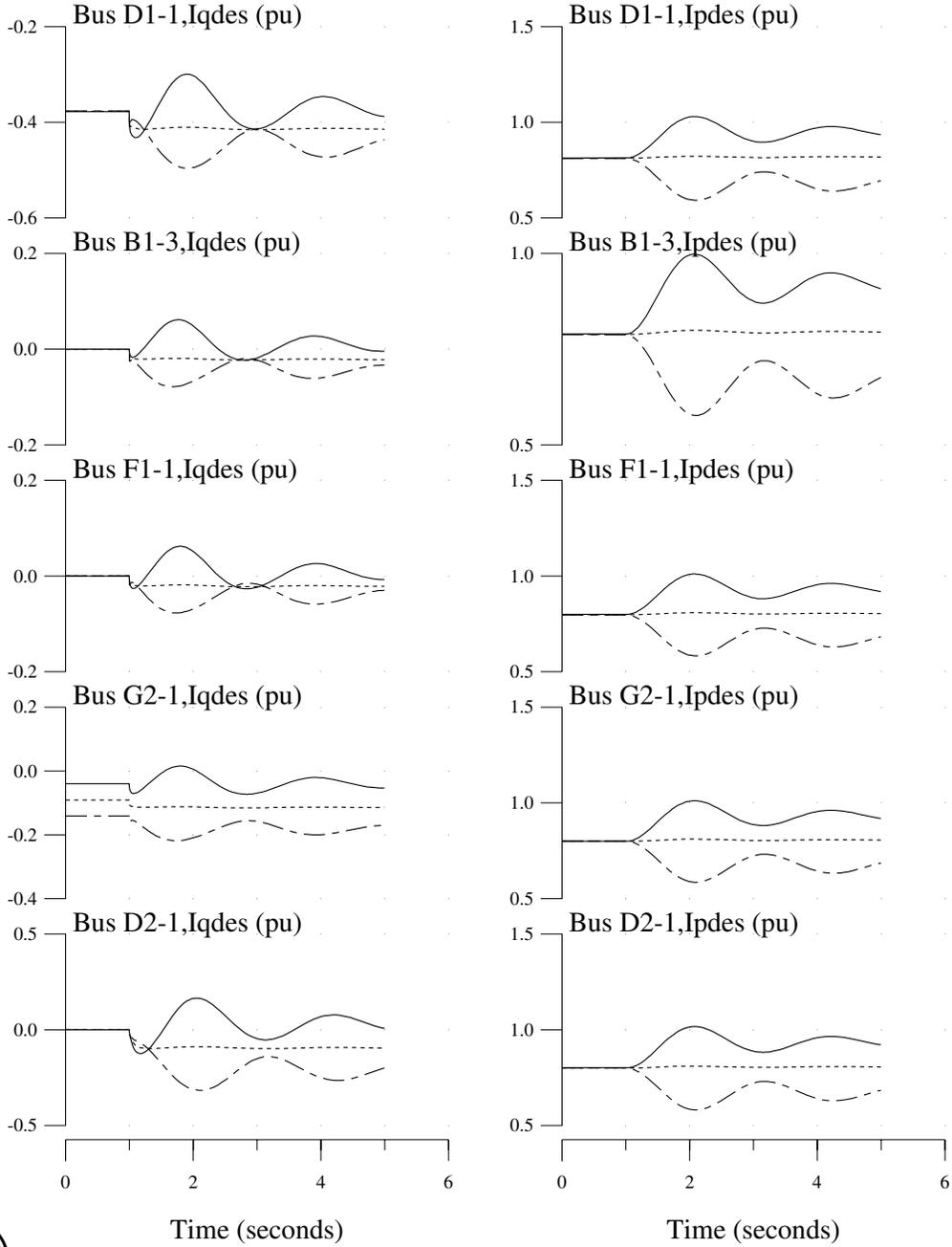
## System 2: Frequency Regulation DG Active and Reactive Power

Initial power from the external grid +2MW(\_\_\_\_),+1MW(- -),+0MW(\_\_\_\_),-1MW(\_\_\_\_),isl(\_\_\_\_)



## System 2: Frequency Regulation DG Control signals

Initial power from the external grid +2MW(\_\_\_\_),+1MW(- -),+0MW(\_\_\_\_),-1MW(\_\_\_\_),isl(\_\_\_\_)



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## SEPARATOR 2: P2 SYSTEM CONFIGURED AS A MICRO GRID

All Inverter Based DGs with Voltage and Frequency Regulation  
Response to Trip of Microgrid from the Utility Grid

*This is the same case as shown in the previous group of traces, except that the **unstable** case with initial import of 2 MW is included. Note the change in scales, and trace patterns.*

4 Cases on Each Set of Axes reflect different initial power exchanges with the utility grid:

Solid Trace: Microgrid Initially Importing approximately 2 MW.

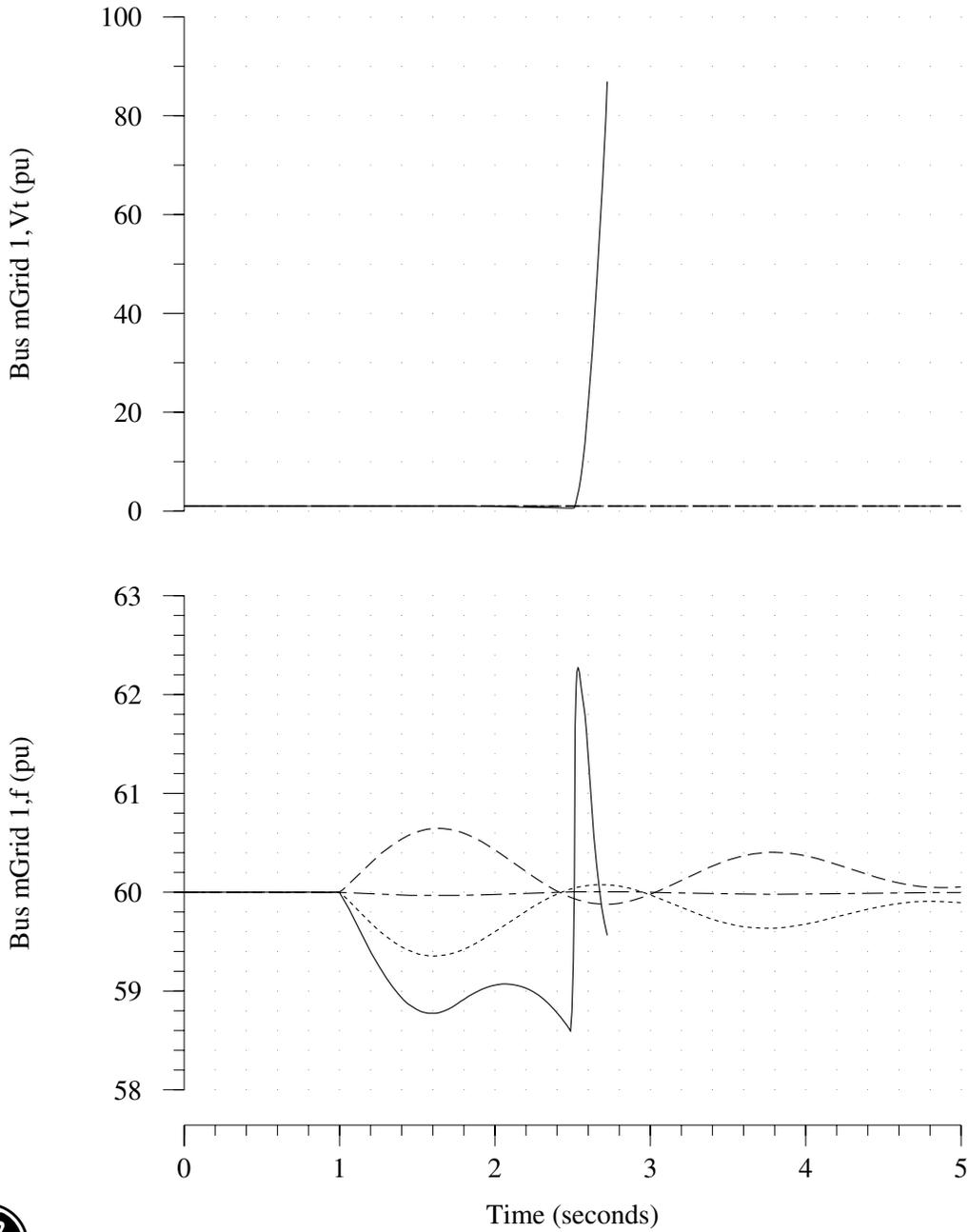
Dotted Trace: : Microgrid Initially Importing approximately 1 MW.

Dot-Dash Trace: Microgrid Initially nearly balanced (very small import)

Dash Trace: Microgrid Initially Exporting approximately 1 MW

### System 2: Frequency Regulation System Quantities

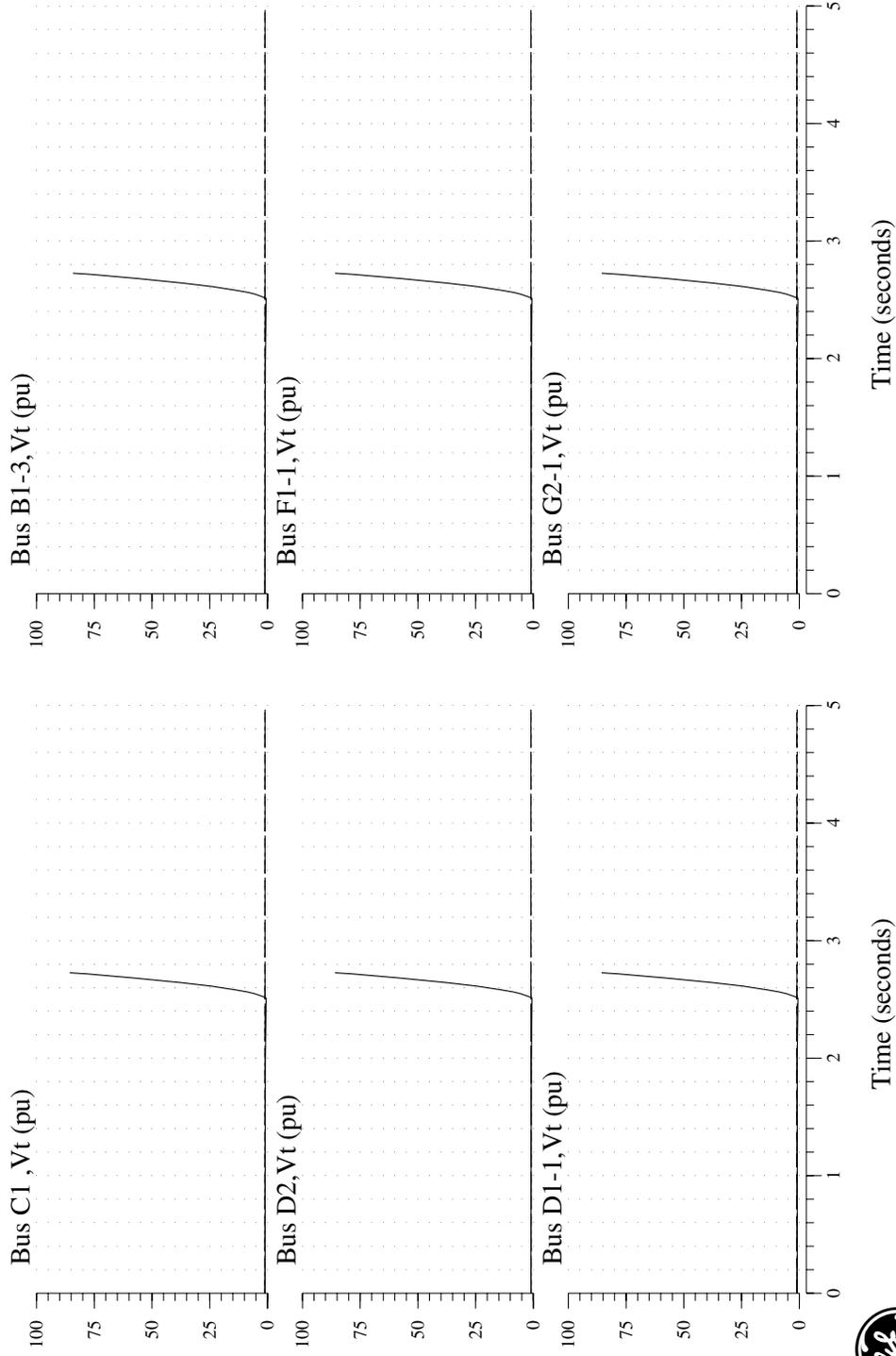
Initial power from the external grid +2MW(\_\_\_\_),+1MW(- -),+0MW(\_\_\_\_),-1MW(\_\_\_\_),isl(\_\_\_\_)



## System 2: Frequency Regulation

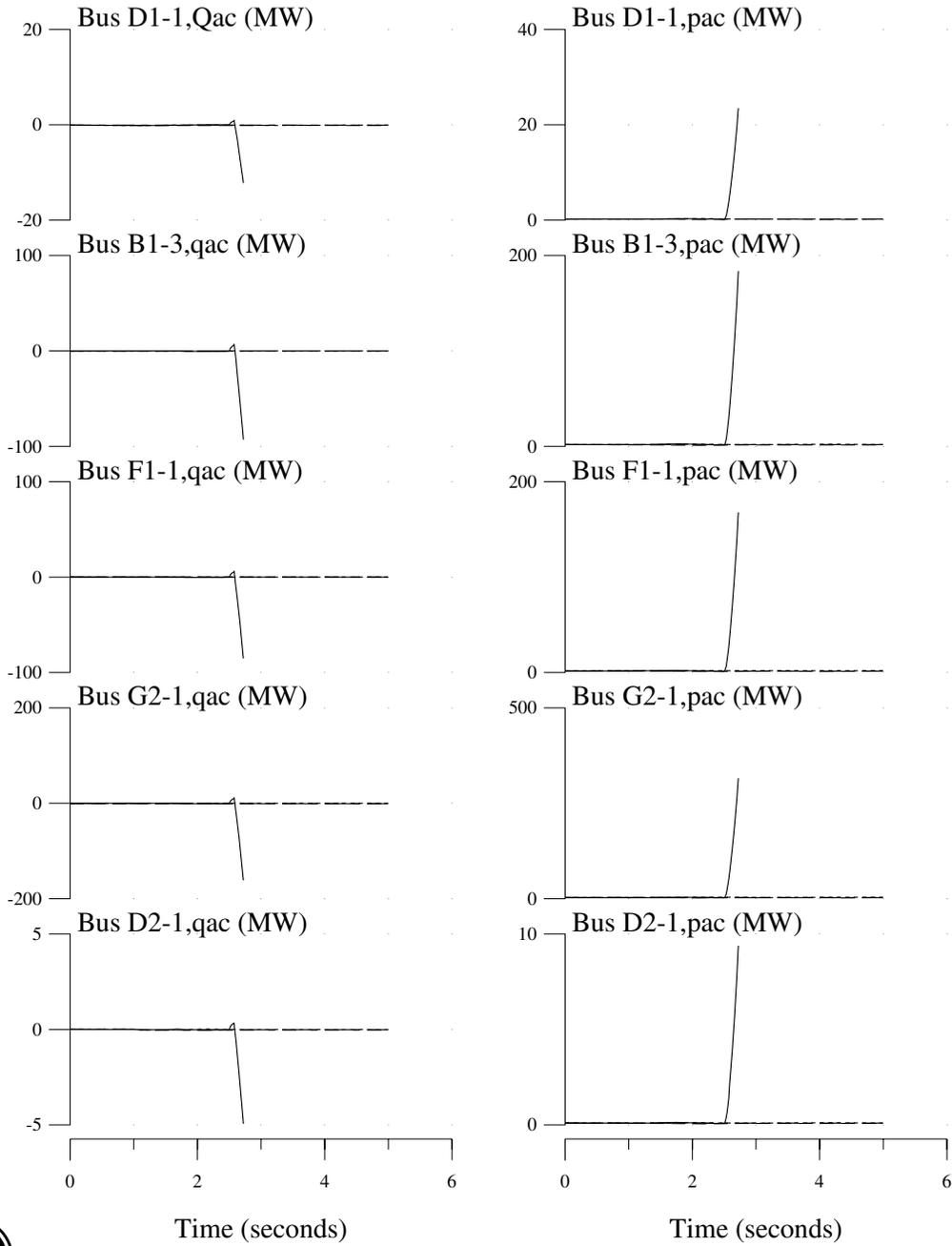
### Voltages

Initial power from the external grid +2MW(\_\_\_\_),+1MW(- -),+0MW(\_\_\_\_),-1MW(\_\_\_\_),isl(- - -)



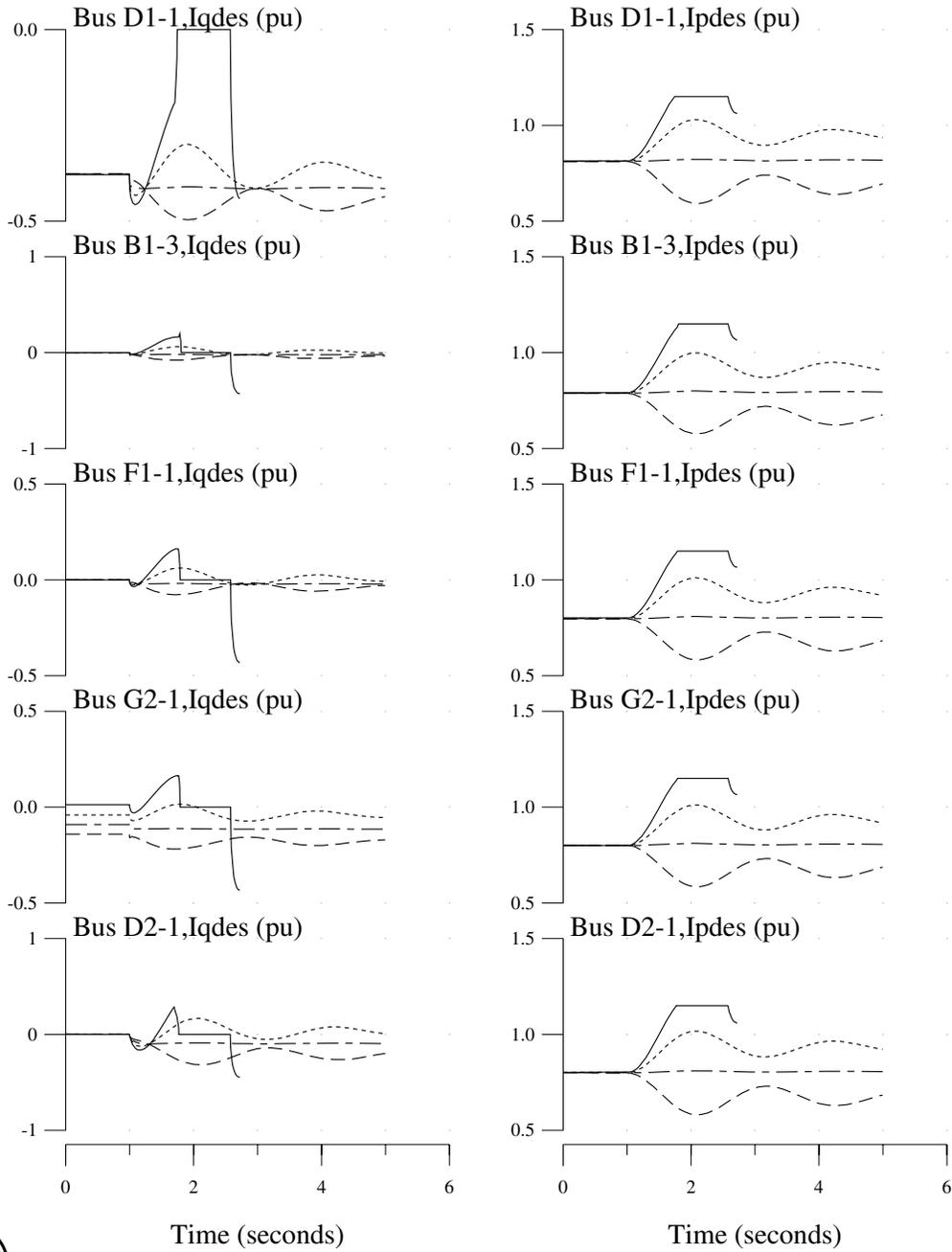
## System 2: Frequency Regulation DG Active and Reactive Power

Initial power from the external grid +2MW(\_\_\_\_),+1MW(- -),+0MW(\_\_\_\_),-1MW(\_\_\_\_),isl(\_\_\_\_)



## System 2: Frequency Regulation DG Control signals

Initial power from the external grid +2MW(\_\_\_\_),+1MW(- -),+0MW(\_\_\_\_),-1MW(\_\_\_\_),isl(\_\_\_\_)



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**SEPARATOR 3: P2 SYSTEM CONFIGURED AS A MICRO GRID**

All Inverter Based DGs with Voltage and Frequency Regulation  
Response to Trip of a Load on the Microgrid

5 Cases on Each Set of Axes reflect different initial power exchanges with the utility grid:

Solid Trace: Microgrid Initially Importing approximately 2 MW.

Dotted Trace: : Microgrid Initially Importing approximately 1 MW.

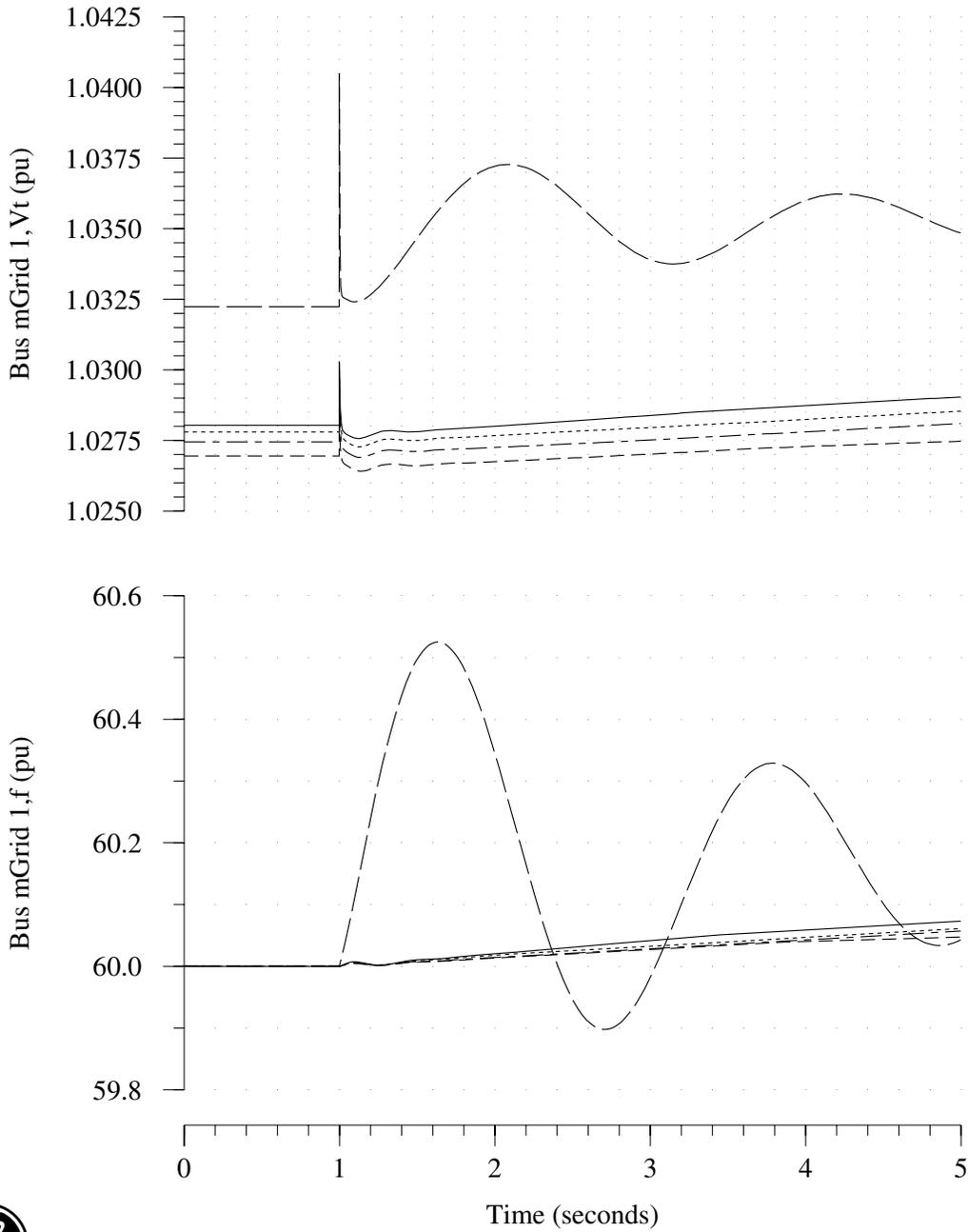
Dot-Dash Trace: Microgrid Initially nearly balanced (very small import)

Dash Trace: Microgrid Initially Exporting approximately 1 MW

Long Dash: Microgrid Initially Operating Islanded from the Grid

### System 2: Frequency Regulation System Quantities

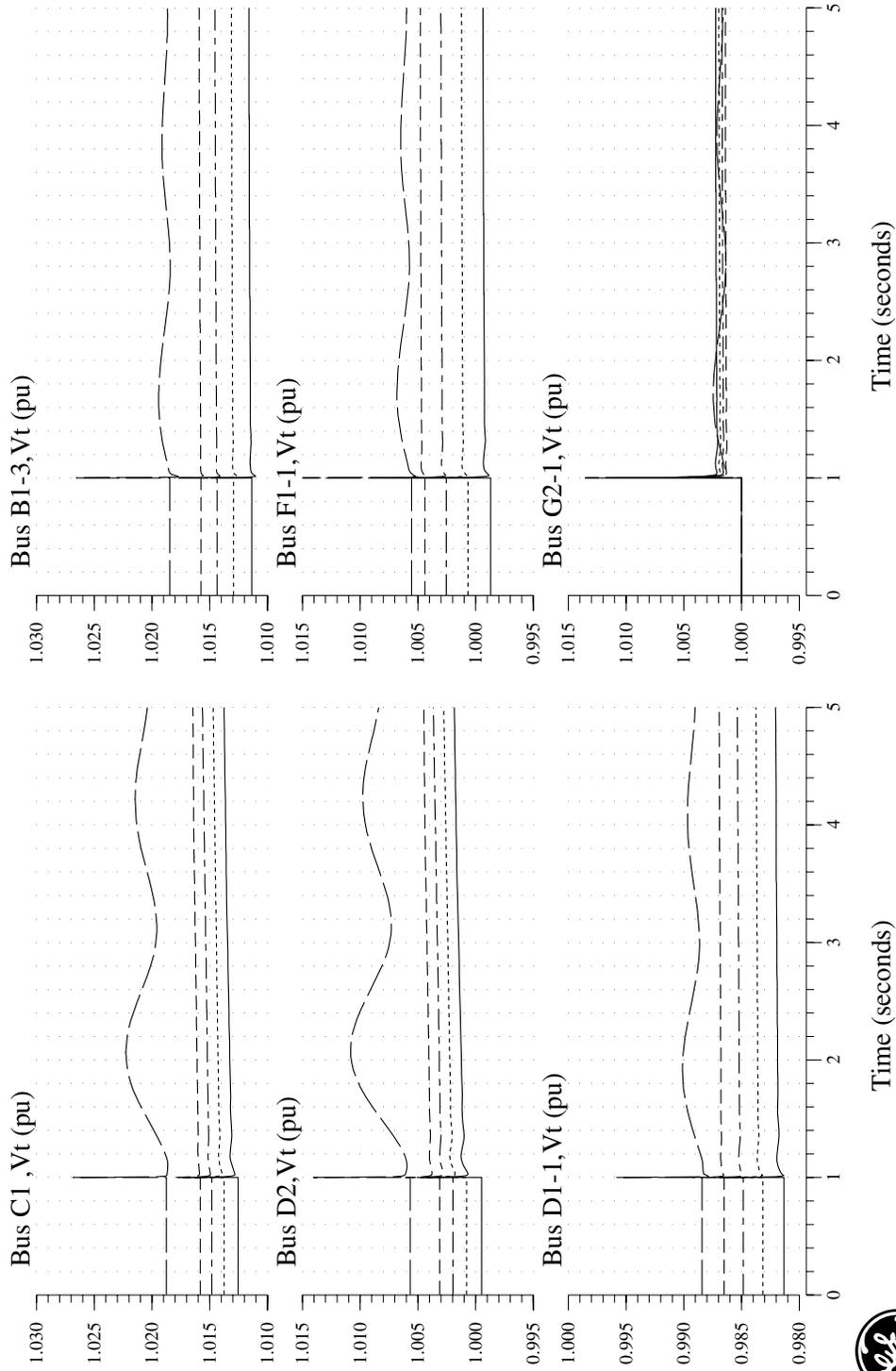
Initial power from the external grid +2MW(\_\_\_\_),+1MW(- -),+0MW(\_\_\_\_),-1MW(\_\_\_\_),isl(\_\_\_\_)



## System 2: Frequency Regulation

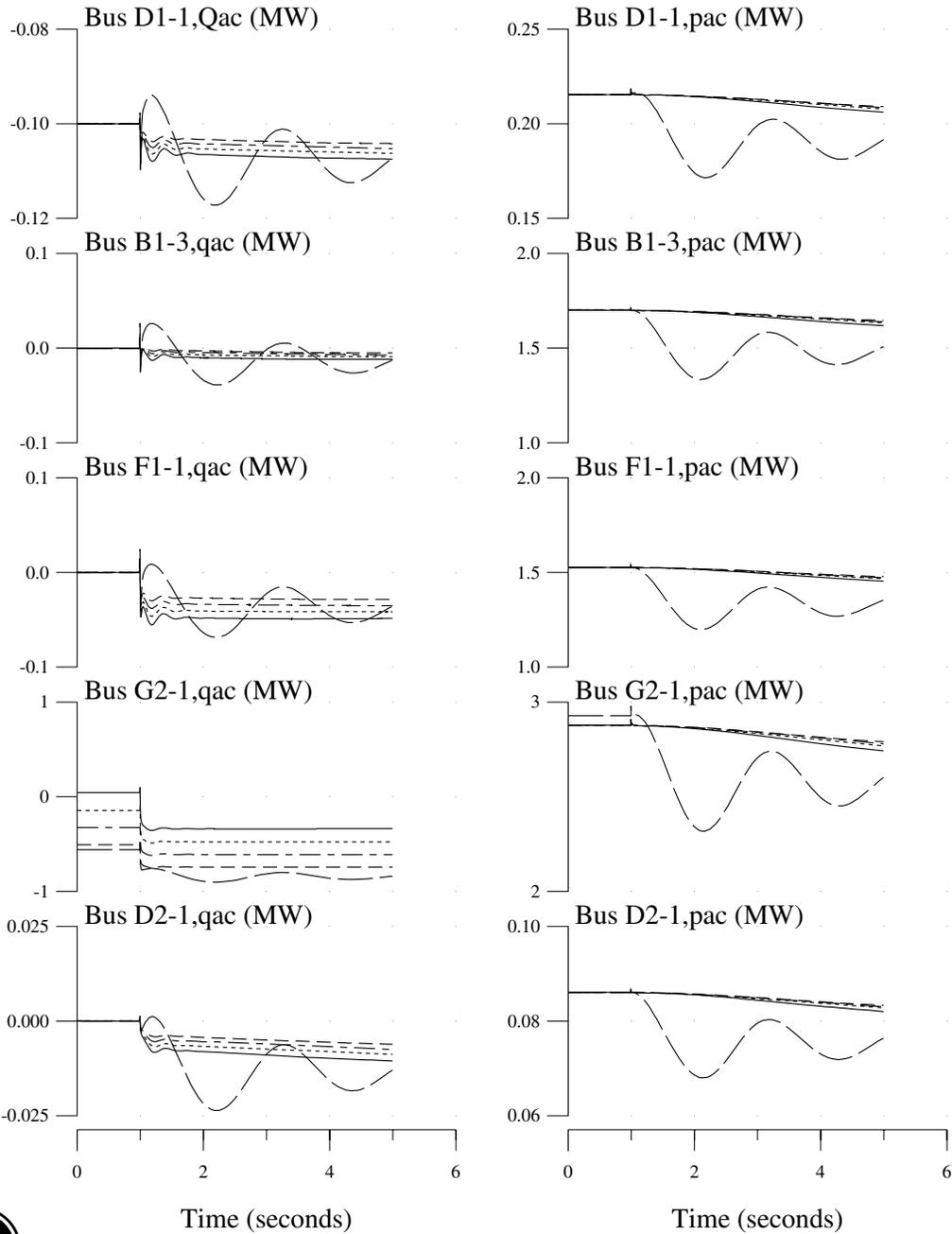
### Voltages

Initial power from the external grid +2MW(\_\_\_\_),+1MW(- -),+0MW(\_\_\_\_),-1MW(\_\_\_\_),isl(- -)



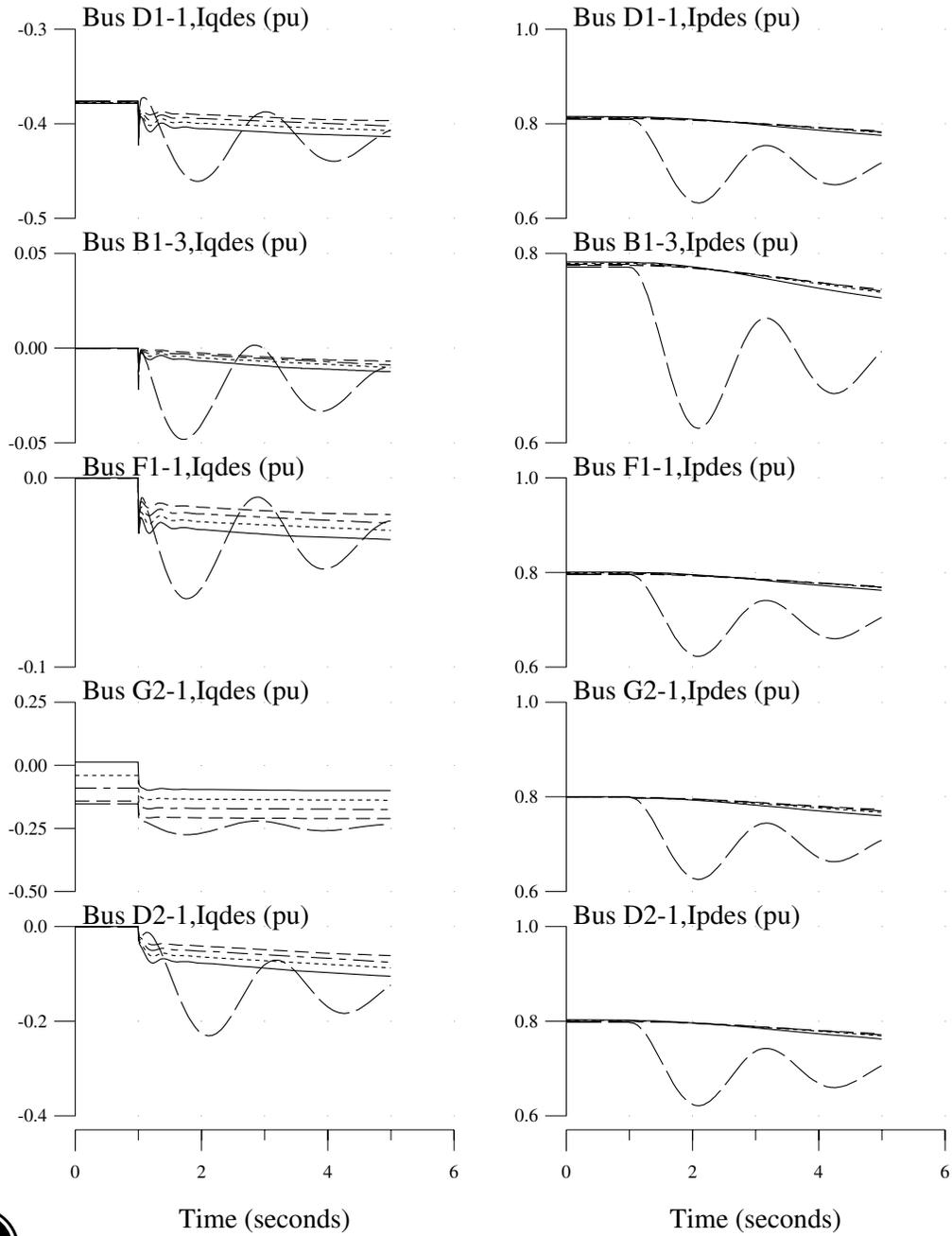
## System 2: Frequency Regulation DG Active and Reactive Power

Initial power from the external grid +2MW(\_\_\_\_),+1MW(- -),+0MW(\_\_\_\_),-1MW(\_\_\_\_),isl(\_\_\_\_)



## System 2: Frequency Regulation DG Control signals

Initial power from the external grid +2MW(\_\_\_\_),+1MW(- -),+0MW(\_\_\_\_),-1MW(\_\_\_\_),isl(\_\_\_\_)



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**SEPARATOR 4: P2 SYSTEM CONFIGURED AS A MICRO GRID**

All Inverter Based DGs with Voltage and Frequency Regulation  
Response to Trip of a DG on the Microgrid

4 Cases on Each Set of Axes reflect different initial power exchanges with the utility grid:

Solid Trace: Microgrid Initially Importing approximately 2 MW.

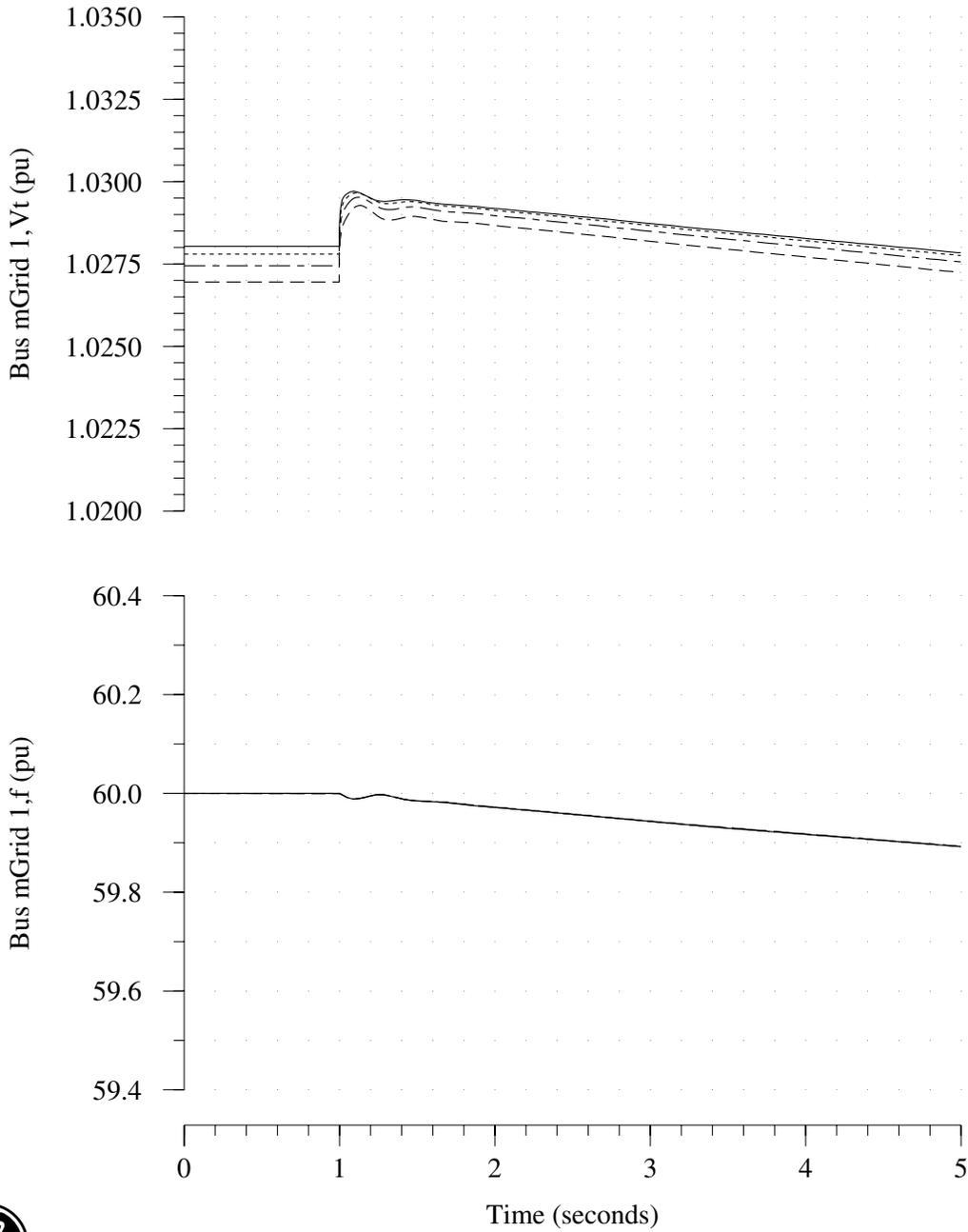
Dotted Trace: : Microgrid Initially Importing approximately 1 MW.

Dot-Dash Trace: Microgrid Initially nearly balanced (very small import)

Dash Trace: Microgrid Initially Exporting approximately 1 MW

### System 2: Frequency Regulation System Quantities

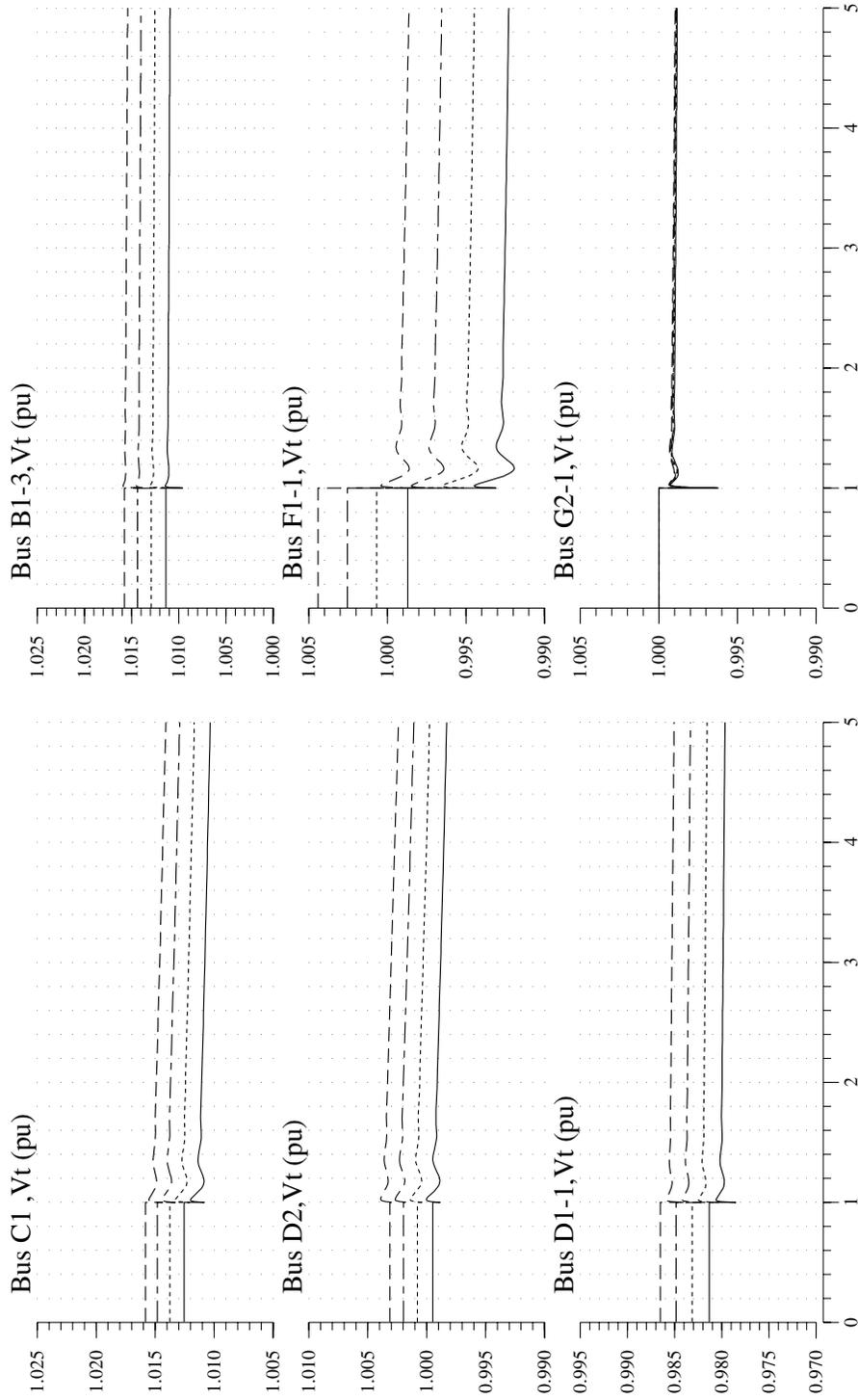
Initial power from the external grid +2MW(\_\_\_\_),+1MW(- -),+0MW(\_\_\_\_),-1MW(\_\_\_\_),isl(\_\_\_\_)



# System 2: Frequency Regulation

## Voltages

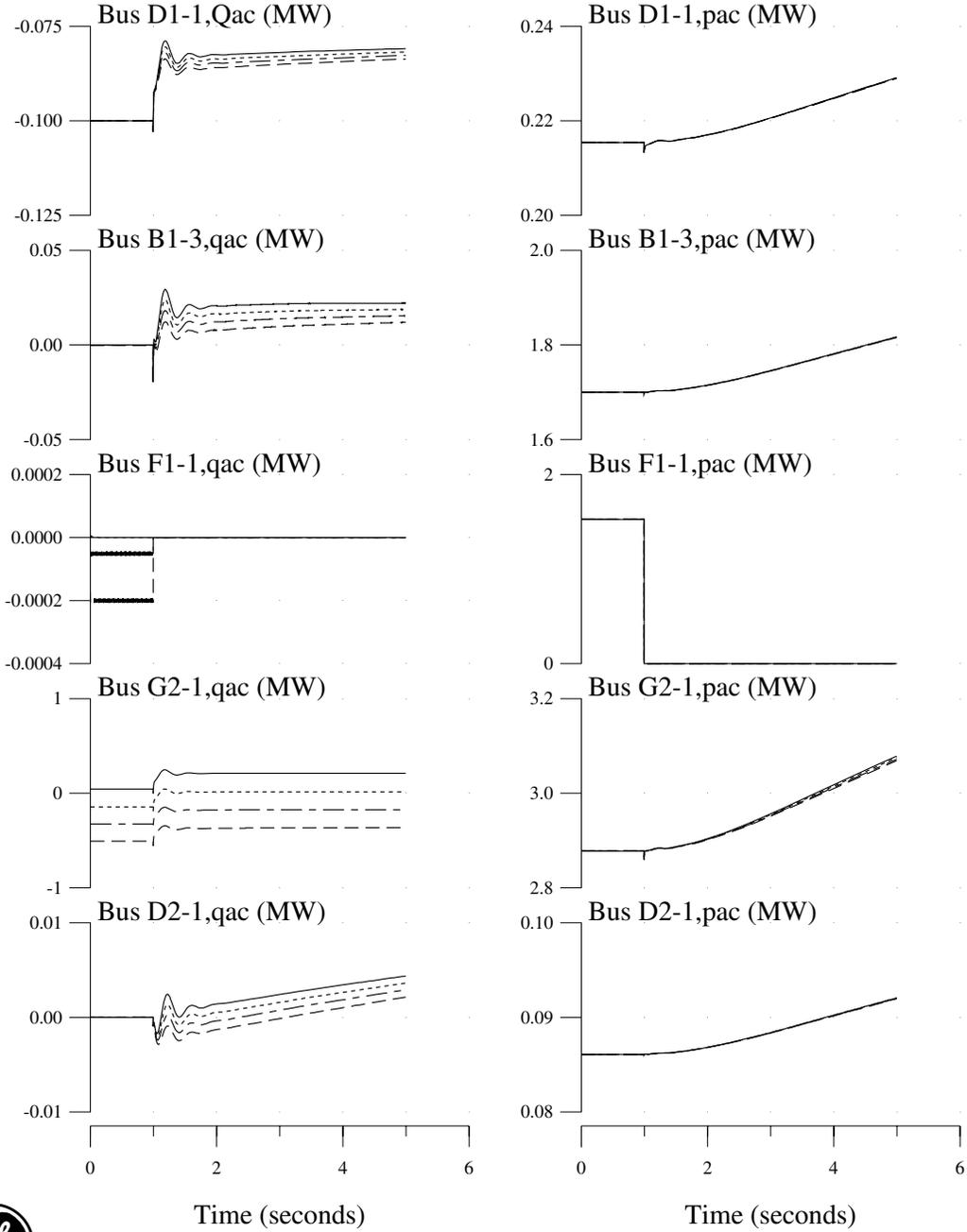
Initial power from the external grid +2MW(\_\_\_\_),+1MW(- -),+0MW(\_\_\_\_),-1MW(\_\_\_\_),isl(- - -)



Time (seconds)

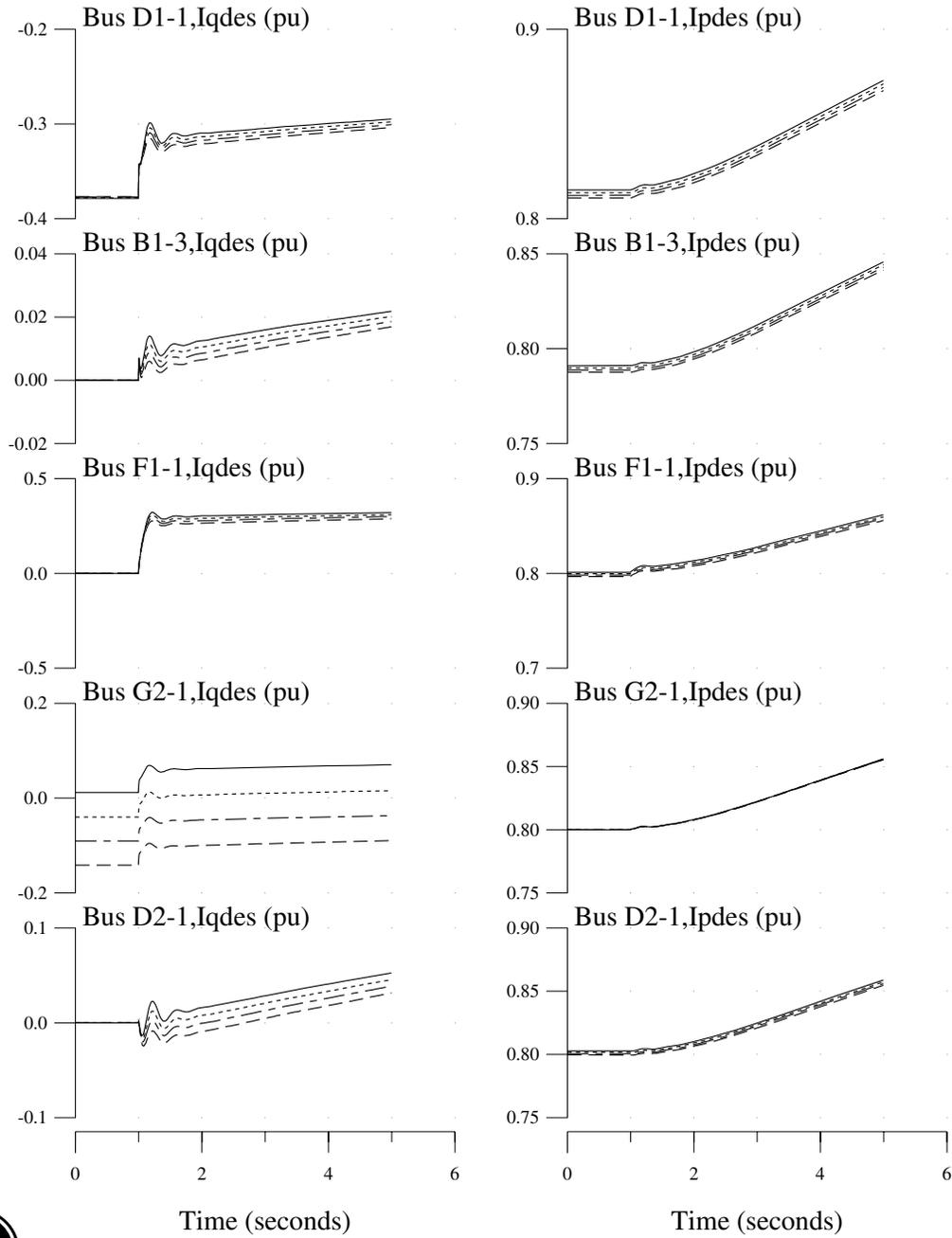
## System 2: Frequency Regulation DG Active and Reactive Power

Initial power from the external grid +2MW(\_\_\_\_),+1MW(- -),+0MW(\_\_\_\_),-1MW(\_\_\_\_),isl(\_\_\_\_)



## System 2: Frequency Regulation DG Control signals

Initial power from the external grid +2MW(\_\_\_\_),+1MW(- -),+0MW(\_\_\_\_),-1MW(\_\_\_\_),isl(\_\_\_\_)



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**SEPARATOR 5: P2 SYSTEM CONFIGURED AS A MICRO GRID WITH SUPERVISORY CONTROL**

All Inverter Based DGs with Voltage and Frequency Regulation  
Response to Trip of a Load on the Microgrid

First Page - 2 Traces:

Green Trace: System Frequency

Red Trace: Active Power of DG on bus D2

Second Page – 2 Traces:

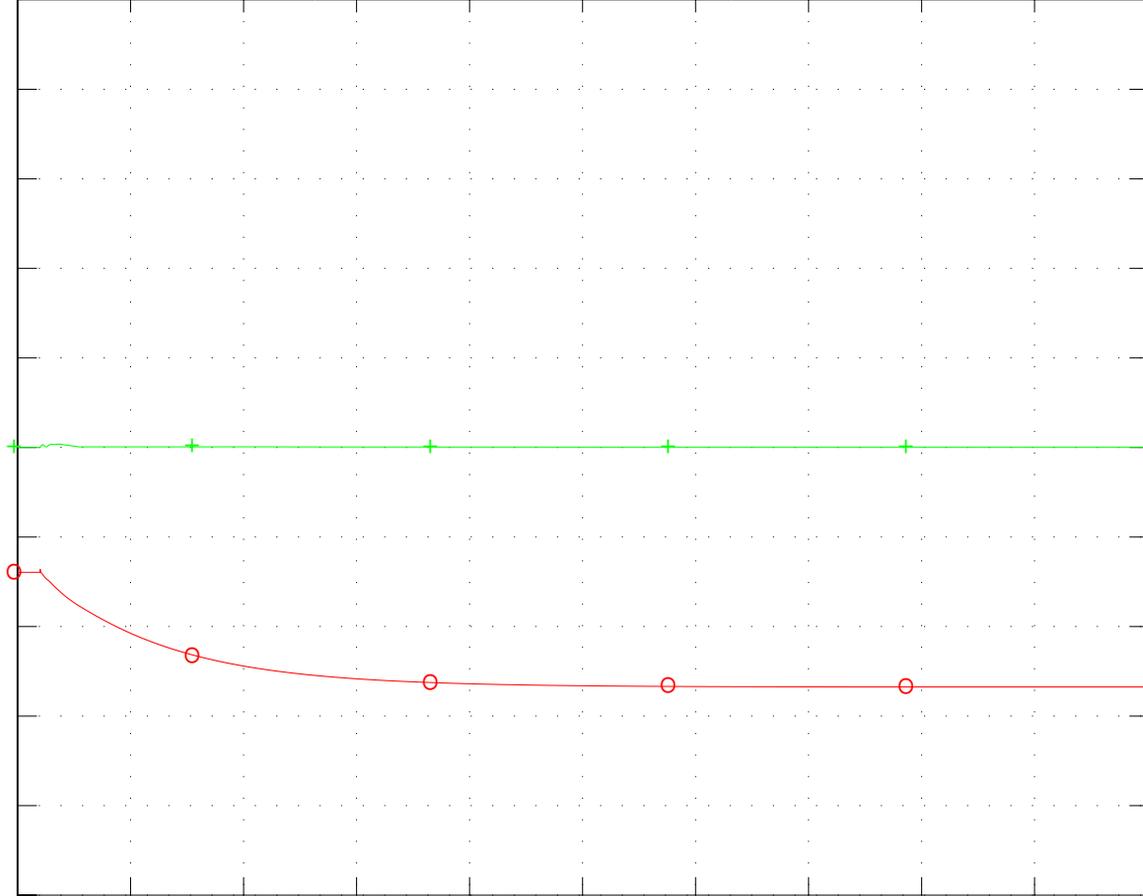
Green Trace: Bus Voltage

Red Trace: Reactive Power of DG on bus D2



label1  
Mon Sep 17 11:01:45 2001

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d:\dg\nrel\p2sys\agc\nrel-mgrid5+1.sav



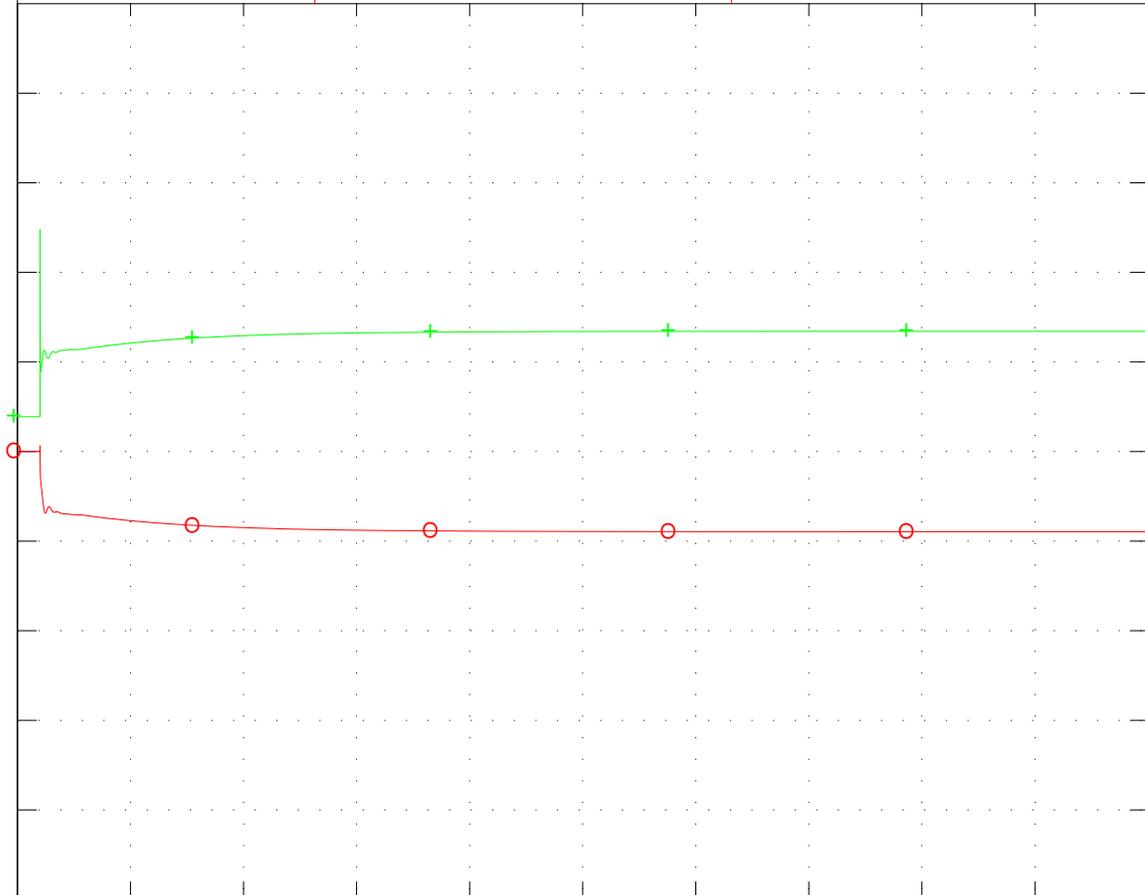
0.00000							50.00000
0.0500		O	pac	2041 D2-1	0.24 pa	1	0.1500
59.000		+	fbus	100 mGrid 1	12.50	1	61.000

Load Trip  
System 2  
Trip loads at buses 201 and 2071



label1  
Mon Sep 17 11:02:00 2001

d:\dg\nrel\p2sys\agc\agc.chf  
d:\dg\nrel\p2sys\agc\nrel-mgrid5+1.sav



0.00000								50.0000
-0.050		o	qac	2041 D2-1	0.24	qa	1	0.0500
0.9900		+	vbus	204 D2	12.50		1	1.0100

Load Trip  
System 2  
Trip loads at buses 201 and 2071